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# A Controllable Voltage Equalizer with State of Charge Prediction for Supercapacitors in Large Current Applications ⋆

**Liran Li** *,** **Zhiwu Huang** *,** **Weirong Liu** *,** **Hao Li** *,**
**Heng Li** *,** **Yingze Yang** *,**

* *School of Information Science and Engineering,Central South University, Changsha, HUNAN 410075 China (e-mail: hzw@csu.edu.cn)*
** *Hunan Engineering Laboratory for Advanced Control and Intelligent Automation Changsha, Hunan, 410075, China*

**Abstract:** The voltage imbalance of cells will reduce supercapacitor stack storage efficiency, and even cause permanent damage. To address this issue, a controllable voltage equalizer with state of charge prediction is proposed in this paper. First, the voltage equalizer is designed by using the controlled multiple-output DC-DC converter to provide a large equalization current. Then, a dynamic linear-recursive model is introduced to predict the state of each supercapacitor. Using the state of charge prediction, a control strategy is proposed to regulate the cells' charging current. The proposed voltage equalizer can obtain the complete balance of capacitor voltage in large current applications. The simulation and experiment results validate the efficiency of the proposed voltage equalizer.

*Keywords:* Large current application, supercapacitor, voltage equalization, adaptive estimation, state of charge prediction.

## 1. INTRODUCTION

As an emerging energy storage system, supercapacitors (SCs) have many advantages over traditional storage batteries: long life cycle, large charging/discharging capacity, high efficiency, fast dynamic response. It is therefore becoming the most attractive energy-storage device for high-power applications, such as electric vehicles and smart-grid (Y. Zhong et al., 2006; M. Steiner & J. Scholten, 2005).

In many high-power applications, high output voltage of around 900 V or more is needed, thus it is always connecting a series of supercapacitor cells as a stack to satisfy the high-power requirement. However, when the stack of SC cells is charged, cell-voltage imbalance and dispersion may occur because of the different individual cell properties, such as capacitance, internal resistance, self-discharge rate, and environmental conditions (S. Lambert et al., 2010). SCs would not work with full efficiency and even be damaged if the cell-voltage imbalance is not well handled.

Some equalization techniques are usually employed to eliminate such imbalance, and they are mainly classified as the dissipative equalization method and the nondissipative equalization method (Z. G. Kong et al., 2006; J. Cao et al., 2008). Among the dissipative equalization methods, the most common way is to use a switched resistor (A. C. Baughman et al., 2008) or zener diode (D. Linzen et al., 2005) across each capacitor cell in the string, as shown in Fig. 1(a). By utilizing the switching resistor and zener diode regularly, this can bypass the charging current on the cell of large voltage, and achieve the balance without complications. However, in high-power conditions the charging current is high, which will lead to high power losses on resistors, and may damage the SCs due to the high temperature on resistors.

The nondissipative equalization scheme is a good alternative as less power loss is guaranteed. In literature (M. Uno, 2009; C. Speltino, A. Stefanopoulou et al., 2010), a number of flying capacitor equalization schemes are proposed, as shown in Fig. 1(b). The scheme uses a capacitor as an external energy storage device to transfer energy between the stack cells. The advantage of this scheme is its simplicity of circuit topology and control method. However, the equalization current of this scheme is limited by the difference in voltage between the stack capacitors and the flying capacitor.

Another type of equalizer through the series-parallel connection of supercapacitor cells, as shown in Fig. 1(c), has been studied by M. Uno & H. Toyota (2008) because it needs no magnetic components. The drawback in this scheme is similar to that of the flying capacitor scheme in that the equalization current between the capacitors is very low. It will take quite a bit of time to get the voltage balanced and therefore is not suited for high-power applications.

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The equalization scheme based on DC-DC converters is one of the more developed solutions. Such structures always transfer energy from the higher voltage capacitor to the whole stack or to the lower voltage capacitor to avoid over-voltage conditions. The scheme proposed by T. H. Phung et al. (2011) has a high degree of modularity, as shown in Fig. 1(d), since each converter works independently of others. In this circuit, it will take a long time to get equalization, because the energy can only be passed from one cell to an adjacent cell. Therefore, it is not suited for high-power applications. A. Xu, S. Xie & X. Liu (2009) proposed a dynamic voltage equalizer without the voltage-detection and comparative circuits. However, the performance of this scheme is limited by the difference in circuit parameters of each branch.

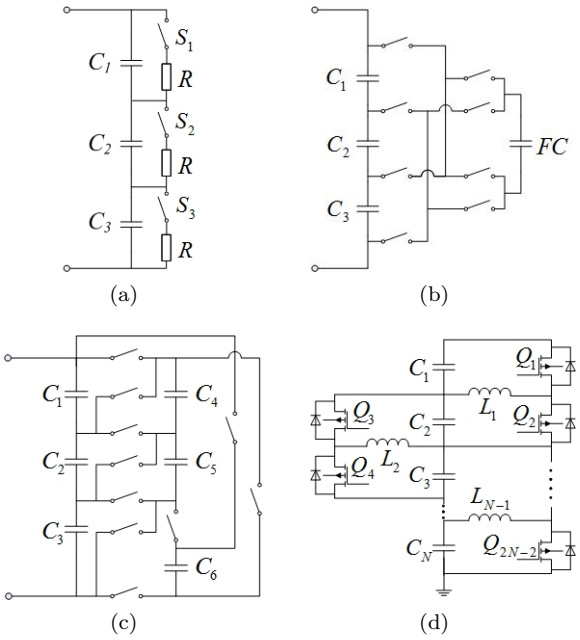


Fig. 1. (a) Switching resistor equalization scheme, (b) Flying capacitor equalization scheme, (c) Series-parallel connection equalization scheme, (d) Buck-boost-based equalization scheme

In high-power applications, the high current will amplify the voltage imbalance effect. To eliminate the effect rapidly, the equalization current must also be high. However, due to the low voltage characteristic of each supercapacitor, the problem of how to supply high equalization current with the given low voltage still remains.

Moreover, most voltage-equalizing algorithms are always controlled by measuring the voltage of the capacitor, but it can not represent the supercapacitors' real state of charge as the internal resistance shares the same voltage. When the measuring voltages reach consensus, the supercapacitors' real state of charge does not achieve balance due to the differences of internal parameters, especially equivalent series resistance. A method to solve this problem is to estimate the states and internal parameters of supercapacitors and predict the state of charge. The most common method for SoC determination is Coulomb counting (K. S. Ng, C. S. Moo et al.,2009) for its advantage of simple calculation, but it needs accurate measurement of current and enough re-calibration points. C. Jiang et al. (2013) proposed an

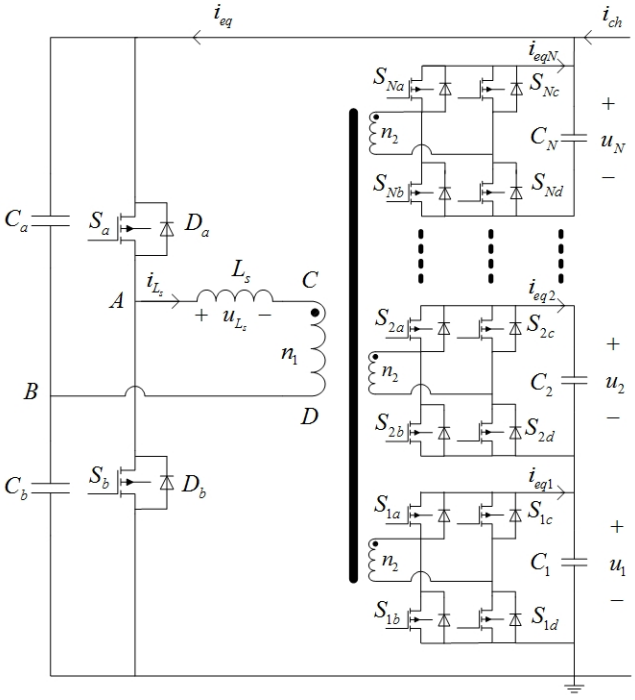


Fig. 2. Voltage-equalization circuit.

Extended Kalman Filter based SoC estimator which could estimate the state of supercapacitors online and reduce the effect of noise on estimation.

In this paper, an improved equalization topology that can offer high equalizing current by using a controllable multiple-output DC-DC converter is proposed. This circuit gets energy from the supercapacitor stack and transfers it to the selected cell by controlling the state of the switches. Since the stack will supply higher voltage than the cell, this scheme will produce a higher equalization current compared with other equalization schemes. Then, a linear-recursive model is introduced as the model of supercapacitors. Making use of this model, the supercapacitors' behavior can be predicted. It will help the controller predict the weakest cell. By using the recursive least squares method, the model parameter could be estimated and updated live.

## 2. EQUALIZATION CIRCUIT

The framework of the voltage-equalizing circuit is shown in Fig. 2. The equalizing circuit can be seen as a controlled multiple-output DC-DC converter. The secondary side voltage of the transformer can be regulated a little higher than the average voltage of the cells by selecting the parameters of the circuit. When the voltage-equalizing circuit is active, a large current will be generated to charge the stack by opening a corresponding MOSFET. Moreover, the reverse parallel diodes in the other branch make the voltage on the secondary side not large enough to open, so the equalizing current is only generated in the branch where the MOSFET is on. By controlling the work status of MOSFET in different branches to change the charging current, the voltage of supercapacitors can eventually achieve consensus.

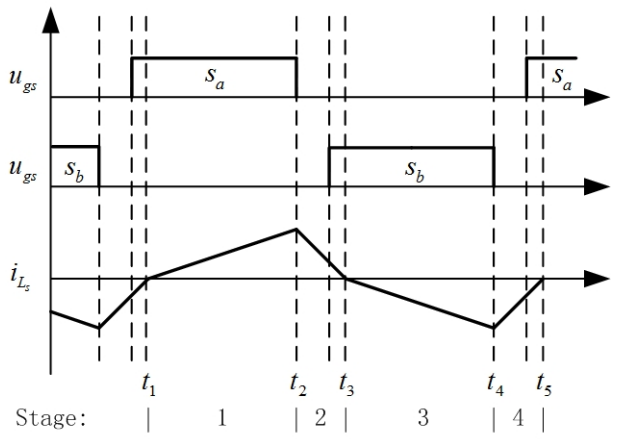


Fig. 3. Equalization circuit mode.

For simplification, it is assumed that the switching tubes, inductances and capacitors are all ideal devices. The leakage inductance of the transformer is represented as $L_s$. It is also assumed that there are $N$ supercapacitor cells in a stack, where the cell capacitance is $C_n(n = 1, 2 \ldots, N)$, the cell voltage is $u_n(n = 1, 2 \ldots, N)$, the stack voltage is $u_{array}$, the stack charging current is $i_{ch}$, the ratio of the transformer is $K = n_1 : n_2$, and the switching frequency of the half-bridge converter is $f_s = 1/T_s$. It is further assumed $u_{array}$ stays fixed during the switching period.

When the circuit is active, the conducting time of switching tubes $S_a$ and $S_b$ will influence the equalization current. When $S_a$ and $S_b$ switch at a duty ratio of 50%, the equalization current will reach its maximum. As shown in Fig. 3, the equalization circuit mode is analyzed as follows:

Stage 1: When $S_a$ turns on and $S_{1a}$, $S_{1d}$ also turn on, resulting in:

$$\begin{aligned} u_{AB} &= \frac{1}{2}u_{array} \\ u_{CD} &= K \cdot u_1 \\ u_{L_s} &= u_{AB} - u_{CD} = \frac{1}{2}u_{array} - K \cdot u_1 \end{aligned} \tag{1}$$

At stage 1, both current of leakage inductance $i_{L_s}$ and the secondary current $i_{eq1}$ increase and the supercapacitor $C_1$ is charging. At time $t_2$, the current of leakage inductance reaches its maximum:

$$i_{L_s max} = \left(\frac{1}{2}u_{array} - K \cdot u_1\right) \cdot (t_2 - t_1)/L_s \tag{2}$$

Stage 2: At time $t_2$, Sa turns off and $S_{1a}$, $S_{ad}$ turn off, the leakage current flows through the antiparallel diode $S_b$, which results in the following:

$$\begin{aligned} u_{AB} &= -\frac{1}{2}u_{array} \\ u_{CD} &= K \cdot u_1 \\ u_{L_s} &= u_{AB} - u_{CD} = -\frac{1}{2}u_{array} - K \cdot u_1 \end{aligned} \tag{3}$$

At stage 2, $i_{L_s}$ decreases rapidly, but still charge the least capacitor until the current decreases to zero. Then $S_{1a}$,$S_{1d}$ turns off, resulting in:

$$i_{L_s max} = \left(\frac{1}{2}u_{array} + K \cdot u_1\right) \cdot (t_3 - t_2)/L_s \tag{4}$$

Stage 3: when both $s_b$ and $s_{1b}$ $s_{1c}$ turn on, the current of leakage inductance will increase at the same rate as in Stage 1 and reach its maximum at time $t_4$, thus

$$\begin{aligned} u_{AB} &= -\frac{1}{2}u_{array} \\ u_{CD} &= -K \cdot u_1 \\ u_{L_s} &= u_{AB} - u_{CD} = -\frac{1}{2}u_{array} + K \cdot u_1 \end{aligned} \tag{5}$$

Stage 4: When $s_b$ turns off and $s_{1b}$, $s_{1c}$ turns on, the leakage current flows trough the antiparallel diode of $s_a$ resulting in the following:

$$\begin{aligned} u_{AB} &= \frac{1}{2}u_{array} \\ u_{CD} &= -K \cdot u_1 \\ u_{L_s} &= u_{AB} - u_{CD} = \frac{1}{2}u_{array} + K \cdot u_1 \end{aligned} \tag{6}$$

When the leakage current returns to zero, $s_{1b}$, $s_{1c}$ turn off. Then $s_a$ will do its work in the next period.

The scheme proposed in this paper is similar to the circuit proposed by A. Xu, S. Xie & X. Liu (2009), but the primary difference is that a MOSFET is used in a rectified circuit connected with the secondary side of transformer instead of a diode. Due to the lower initial resistance, a higher equalizing current could be provided in the same voltage to reduce the charging time. If the circuit still uses diodes, the equalizing result will be constrained by the component consensus of all equalizing circuit branches. The equalized voltages also have differences among cells due to the differences among components. On the contrary, with MOSFET, each branch can be controlled solely to reduce the dependence on component features and obtain a better robustness and equalizing result.

In the equalization circuit, the equalization current $i_{eqn}$ plays an important role in the equalization rate. In this circuit:

$$i_{eqn} = \frac{1}{2}i_{L_s \max} \cdot K \qquad u_{array} = N \cdot u_{eq} \tag{7}$$

where $u_{eq}$ is the average voltage of a supercapacitor stack. Summarizing the above equations, the branch current is

$$i_{eqn} = a + b \cdot u_{ern} + c \cdot u_{ern}^2 \tag{8}$$

where

$$\begin{aligned} a &= \frac{KT(N^2 - 4K^2)}{8LN}u_{eq}, b = \frac{K^3 T}{LN}, \\ c &= -\frac{k^3 T}{2LNu_{eq}}, u_{ern} = u_{eq} - u_n. \end{aligned} \tag{9}$$

where $u_{ern}$ is the difference between the average voltage and the cell voltage. From the above equation, it can be seen that the closer the cell voltage reaches the average voltage, the lower the current will be. In order to ensure a high enough equalization current, the turn ratio of the transformer should be chosen as $K < 0.5N$. At the same time, the leakage inductance $L_s$ of the transformer and the switching frequency of MOSFET will have a great influence on the equalization current. The lower leakage inductance $L_s$ and switching frequency ,the higher the equalization current.

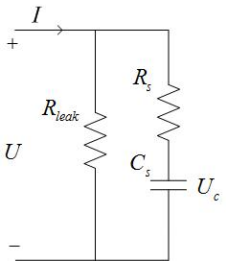


Fig. 4. Supercapacitor equivalent circuit model.

## 3. STATE PREDICTION AND CONTROL SCHEME

The previous equalization circuit can be treated as a multiple-output DC-DC converter. In order to control its output state and equalize the voltage of supercapacitors, it is required to measure the state of supercapacitors and construct a closed loop. Existing supercapacitor equalization systems typically rely on the measured voltage. The key process is to transfer the energy to a low voltage cell or from a high voltage cell. By repeating the process, the increased rates of all supercapacitors remain the same and the voltage is equalized. However, in practical applications, due to the internal parameters' difference, especially the internal resistance, the measured voltage cannot represent the real charging state; this may causes the energy transformation among cells repeatedly and thus leads to unmeaning energy consumption. In order to predict the accurate charging state, a first-order circuit is used as the equivalent model of supercapacitors, as shown in Fig. 4.

In the circuit, $U$ is the capacitor voltage, $I$ is the charging current, $R_{leak}$ is the leakage resistance, $R_s$ and $C_s$ are the resistances and capacitances of the branch respectively. The voltage of $C_s$ can treated as the real charging voltage of supercapacitors. The transform function of the model is represented as

$$U_c = (\frac{R_{leak}+R_s}{R_{leak}})U - IR_s \tag{10}$$

In order to calculate $U_c$ with the above equation, it is necessary to identify parameters of the equivalent model. In this paper, the least squares method is adopted to identify parameters of the model. The procedure is:

1. Design the transform function of the equivalent circuit model:

$$G(s) = \frac{U(s)}{I(s)} = \frac{R_{leak}R_sC_ss + R_{leak}}{(R_{leak}+R_s)C_ss+1} \tag{11}$$

2. Derive the discrete time transform function and recurrence formula. Let

$$s = \frac{2(1-z^{-1})}{T(1+z^{-1})} \tag{12}$$

then the discrete time transform function and recurrence formula is as follows:

$$G(z^{-1}) = \frac{U(z^{-1})}{I(z^{-1})} = \frac{a_2+a_3z^{-1}}{1-a_1z^{-1}} \tag{13}$$

$$U(k) = a_1U(k-1) + a_2I(k) + a_3I(k-1) \tag{14}$$

3. Construct the linear discrete time model:

In (14), parameters $a_1$,$a_2$,$a_3$ are unknown variables. Equation (14) is rewritten as follows

$$U(k) = h^T(k)\theta + e(k) \tag{15}$$

in which $e(k)$ represents the sampling error at time $k$ and

$$\begin{aligned} &h^T(k) = [U(k-1), I(k), I(k-1)] \\ &\theta = [a_1, a_2, a_3]^T \end{aligned} \tag{16}$$

4. Estimate unknown variables using the least squares method:

$\hat{\theta}_{LS}$ is denoted as the estimate of $\theta$, therefore the recurrence least squares algorithm is denoted as follows:

$$\begin{aligned} &\hat{\theta}_{LS}(k) = \hat{\theta}_{LS}(k-1) + K(k)\theta(k) \\ &\theta(k) = U(k) - h^T(k)\hat{\theta}_{LS}(k-1) \\ &K(k) = \frac{P(k-1)h(k)}{1+h^T(k)P(k)h(k)} \\ &P(k) = P(k-1) - \frac{P(k-1)h(k)h^T(k)P(k-1)}{1+h^T(k)P(k)h(k)} \end{aligned} \tag{17}$$

5. Solve the equivalent model parameter. Let

$$z^{-1} = \frac{(1-\frac{T}{2}s)}{(1+\frac{T}{2}s)} \tag{18}$$

then the discrete time transform function is denoted as

$$G(s) = \frac{\frac{T(a_2-a_3)}{2(1-a_1)}s + \frac{a_2+a_3}{1-a_1}}{\frac{T(1+a_1)}{2(1-a_1)}s+1} \tag{19}$$

Compared with transform function (11)

$$\begin{cases} R_{leak}R_sC_s = \dfrac{T(a_2-a_3)}{2(1-a_1)} \\ R_{leak} = \dfrac{a_2+a_3}{1-a_1} \\ (R_{leak}+R_s)C_s = \dfrac{T(1+a_1)}{2(1-a_1)} \end{cases} \tag{20}$$

Then the final system parameters are solved to be

$$\begin{cases} R_{leak} = \dfrac{a_2+a_3}{1-a_1} \\ R_s = \dfrac{a_2^2-a_3^2}{2(a_1a_2+a_3)} \\ C_s = \dfrac{T(a_1a_2+a_3)}{(a_2+a_3)^2} \end{cases} \tag{21}$$

When the supercapacitor is in use, it will be charging and discharging repeatedly. Due to the difference in capacitance of each cell, the charging/discharging rate will be different. The smaller capacitance is, the greater voltage changes during the charging/discharging process. If the capacitor cells are charged according to real time status, the energy may be transferred among cells repeatedly and thus lower both the equalization efficiency and the energy utilization.

In order to improve the equalization efficiency, it is necessary to estimate the cell voltage when the Charging process is finished. It is straightforward to estimate the supercapacitors' state by the voltage and current with (14). Then the supercapacitor cells' charging state when the charging is finished can be predicted. Finally, the controller will

control the equalization circuit output according to the prediction result, and achieve the equalization at last. The procedure is:

1. Predict the supercapacitor state using the recurrence formula. Predict the voltage of each supercapacitor when the charging process is finished or the total voltage reaches a certain threshold.

2. Based on the prediction result of step 1, predict the supercapacitor cell with least voltage when the charging process is finished. Then the controller will control the rectifying circuit to give additional charge to the branch.

3. Repeat step 1, when the voltage of the supercapacitor chosen at step 2 reaches the set value, stop charging.

4. Repeat step 1-3, until all cells' voltage predictions reach consensus.

At each step, the least square method is calculated to update and revise the parameters of the recurrence model.

## 4. SIMULATION AND EXPERIMENTS

The simulation is carried out to verify the feasibility of the whole system in the Saber and Matlab/Simulink co-simulation environment. A stack of 4 supercapacitors in series is under consideration. The equalization circuit is simulated by simulation software Saber. Control strategies are implemented by using Matlab/Simulink environment. The two parts are connected by the interface program provided by Saber software.

The parameters of supercapacitor make reference to Maxwell Technologies' K2 series of ultracapacitor cells. The rated capacitance of the supercapacitor is 3000 F. To simulate the parameter's deviation by aging, the capacitance errors are varied from $-10\%$ to $20\%$ in turn. The capacitance values of $C_1$, $C_2$, $C_3$ and $C_4$ are 3600, 3300, 3000 and 2700 F. The charging current is 150 A.

Fig. 5(a) shows the voltages of each capacitor cell and the average current to each capacitor is shown in Fig. 5(b). It is easy to see that the capacitors have the same voltage at last. At the start time of the equalization period, the weakest cell is not charged. The capacitor $C_1$ is charged at first, even though its voltage has a maximum value of the four capacitors. When the capacitor $C_1$'s voltage reaches the proper value, the other capacitors are charged in turn. It's worth noting that, the voltage equalizer does not keep working during the whole charging process. Therefore, this scheme can reduce switching losses of MOSFETs and increase energy efficiency.

A voltage equalization system for connected supercapacitors is set up as shown in Fig. 6. The system is composed of a supercapacitors stack, rectifier circuit, DC-AC circuit and the controller. The supercapacitors stack consists of 8 modules in series, and the rated voltage and capacitance of each module are 2.7 V, 3500 F respectively. The rectifier circuit is made based on double-sided Al substrate to improve the heat dissipation performance, each part of which corresponds to a supercapacitor module separately. The multiple-output transformer on DC-AC circuit is made based on a ferrite core w434-03 with 3 turns in primary winding and 1 turn in each secondary winding. The overall

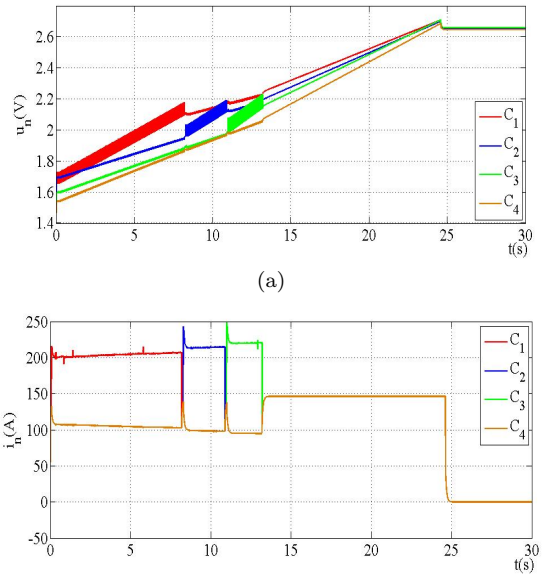


Fig. 5. Simulation results. (a) Voltages of each supercapacitor $u_n$. (b) Average current to each supercapacitor $i_n$.

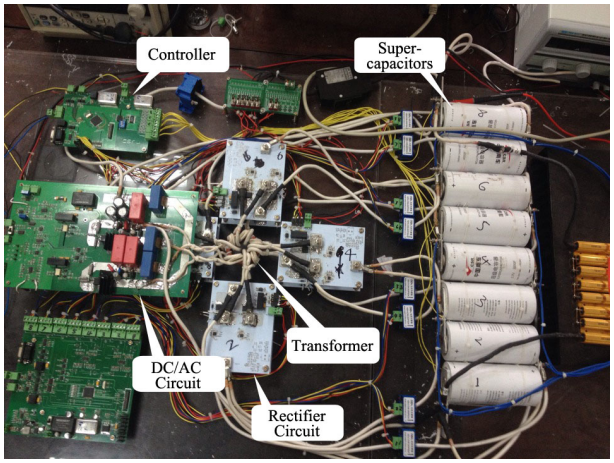


Fig. 6. Voltage equalizer test bench.

control algorithms, the sampling of current, voltage and temperature are implemented on a C166 microcontroller. The switching frequency is set at 10 KHz. The experimental results of the duty ratio and the equalizing current are illustrated in Fig. 7, which shows that the current can reach 80 A.

The most important factor affecting the current output is the inductance of the transformer. In order to conduct large currents, a lot of work had been done during the experiments. To reduce the leakage inductance $L_s$ of the transformer, high-frequency magnetic materials were used and the convert switching frequency reduced from 50 KHz to 10 KHz. The transformer turns ratio was also reduced from 4 to 3 to increase the current driving capability.

## 5. CONCLUSION

In this paper, an improved equalization circuit is proposed to address the problem of voltage imbalance of

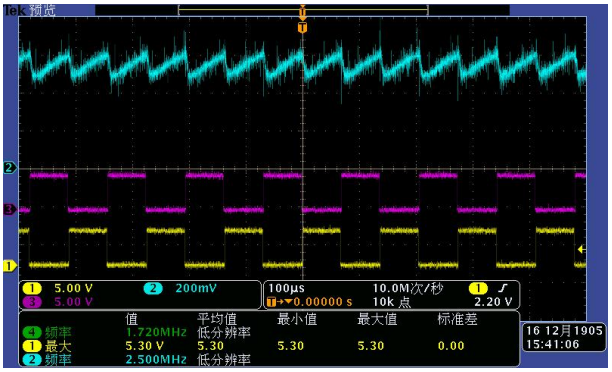


Fig. 7. Equalization current to a supercapacitor.

the connected supercapacitor cells, in which the circuit derives energy from the series supercapacitor stack and transfers it to the specified cell. By utilizing synchronous rectification, this circuit offers high current to achieve fast voltage equalization. A mechanism based on the proposed topology is further introduced to predict the charge state of the supercapacitor to help control the charging current of the cell. This method takes advantage of the characteristic of the supercapacitor cell rather than only considering the output voltage of the cell, and can regulate the charging current of the cell more efficiently and reduce unnecessary power losses on the equalizer. Simulation and experiment results show that the proposed equalization circuit can offer high current satisfactory for high-power situation, and the prediction based control law can achieve the voltage balance precisely and efficiently.

## REFERENCES

Y. Zhong, J. Zhang, G. Li & A. Liu. Research on energy effciency of supercapacitor energy storage system. *Proceedings of IEEE Power System Technology Conference* , 1-4, 2006.

M. Steiner & J. Scholten. Energy storage on board of railway vehicles. *Proceedings of Power Electronics and Applications Conference* , 1-10, 2005.

S. Lambert, V. Pickert, J. Holden, W. Li & X. He. Overview of supercapacitor voltage equalisation circuits for an electric vehicle charging application. *Proceedings of IEEE Vehicle Power and Propulsion Conference* , 1-7, 2010.

Z. G. Kong, C. B. Zhu, R. G. Lu & S. K. Cheng. Comparison and evaluation of charge equalization technique for series connected batteries. *Proceedings of IEEE Power Electronics Specialists Conference* , 1-6, 2006.

J. Cao, N. Schofield & A. Emadi. Battery balancing methods: A comprehensive review. *IEEE Vehicle Power and Propulsion Conference* , 1-6, 2008.

A. C. Baughman & M. Ferdowsi. Double-tiered switched-capacitor battery charge equalization technique. *IEEE Transactions on Industrial Electronics* , 55(6), 2277-2285, 2008.

D. Linzen, S. Buller, E. Karden & R. W. De Doncker. Analysis and evaluation of charge-balancing circuits on performance, reliability, and lifetime of supercapacitor systems. *IEEE Transactions on Industry Applications*, 41(5), 1135-1141, 2005.

C. Speltino, A. Stefanopoulou & G. Fiengo. Cell equalization in battery stacks through state of charge estimation polling. *Proceedings of IEEE American Control Conference*, 5050-5055, 2010.

M. Uno. Series-parallel reconfiguration technique for supercapacitor energy storage systems. *TENCON 2009-2009 IEEE Region 10 Conference*, 1-5, 2009.

M. Uno & H. Toyota. Equalization technique utilizing series-parallel connected supercapacitors for energy storage system. *Proceedings of IEEE Conference on Sustainable Energy Technologies*, 893-897, 2008.

T. H. Phung, J. C. Crebier, A. Chureau, A. Collet & N. T. Van Nguyen. Optimized structure for next-to-next balancing of series-connected lithium-ion cells. *Proceedings of IEEE Applied Power Electronics Conference and Exposition*, 1374-1381, 2011.

A. Xu, S. Xie & X. Liu. Dynamic voltage equalization for series-connected ultracapacitors in EV/HEV applications. *IEEE Transaction on Vehicular Technology*,58(8), 3981-3987, 2009.

K. S. Ng, C. S. Moo, Y. P. Chen & Y. C. Hsieh. Enhanced coulomb counting method for estimating state-of-charge and state-of-health of lead-acid batteries. *Applied energy*, 86(9), 1506-1511, 2009.

C. G. Jiang, A. Taylor, C. Duan & K. Bai. Extended Kalman Filter based battery state of charge (SOC) estimation for electric vehicles. *Proceedings of IEEE Transportation Electrification Conference and Expo* , 1-5, 2013.