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Qualitative Diagnosis Method Based on Process History in Semiconductor Manufacturing Process ⋆

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Abstract: Rapid process diagnosis is a very challenging task for the manufacturing industries in order to maintain the product quality and to reduce the production cost. Process diagnosis became a complex and time-consuming task in semiconductor industries due to the big variability of the products, the long cycle time, the re-entrant flow of the process, the restricted number of controlled lots, and the huge amount of collected data. In order to cope with the complexity and the time-consuming problems, a rapid qualitative diagnosis method based on process history is proposed in this paper. Logic programming is used to describe the algorithm. A prototype has been developed for the defectivity workshop in St-microelectronics and the result shows strong defect source identification and a significant reduction of diagnosis time.

1. INTRODUCTION

Rapid process diagnosis in manufacturing industries consists on quickly detecting the anomalies and identifying their root cause in the process.
Process diagnosis approaches are classified into two classes: Model-based approaches where a priory knowledge of the process is needed, and process history based approaches where only historical process data is needed. See Venkatasubramanian et al. [2003c] and Venkatasubramanian et al. [2003a]. Fig. 1 illustrates the different classes of diagnostic methods.
Based on the input data, methods in process history based approach could be classified into two categories: Quantitative methods such as the expert systems and trend modeling methods, and qualitative methods that are classified as non-statistical or statistical methods. Neural networks are an important class of non-statistical classifiers while Principal component analysis (PCA), partial least squares (PLS), support vector machines (SVM), and statistical pattern classifiers form a major component of statistical feature extraction methods. See Thieullen et al. [2012]. A comparative study of these methods is reported in Venkatasubramanian et al. [2003b] where the authors conclude that no single method has all desirable features.
Semiconductor manufacturing line is a high-mix and low value manufacturing system where more than two hundred products can be concurrently run. The re-entrant flow of the process and the high number of operations increase the cycle time of the products to more than three months.

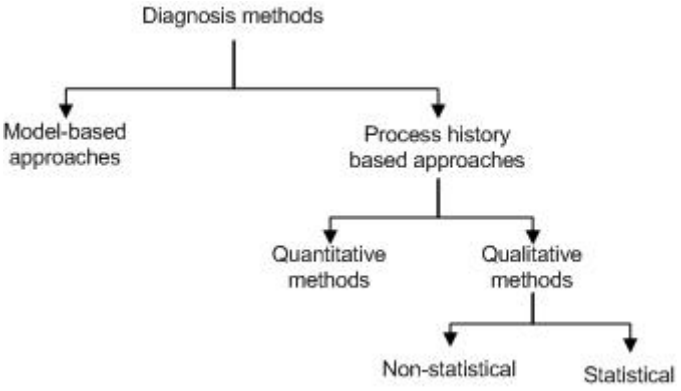

Fig. 1. Classification of diagnostic methods

Terabytes of data are collected every day and stored in databases for the analysis. Products are made in lots of 25 wafers that travel through cluster machines where the wafers are processed simultaneously. Samples of lots are controlled following the control plan during the process while a test is performed at the end on all released lots.
Model-based diagnosis approaches in high-mix manufacturing plant such as semiconductor are limited at the priory knowledge of the new products process. However, a variety of diagnosis approaches based on process history have been developed for the process control. Most of these diagnosis approaches were treating the root cause identification of yield loss event. The proposed methods correlate statistically the end of line control data with the process history data in order to highlight the process step which may cause the yield loss. Yield diagnosis methods are reviewed in Milor [2013]. The insufficient number of controlled lots at the inline control and the long cycle time

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of products to arrive at the end of line control remain the limitations of quantitative diagnosis approaches.
In order to respond to the need of process control in high-mix manufacturing plants, this paper proposes a qualitative process diagnosis method based on the inline control data, to quickly identify the source of defects detected on the controlled lots. At this end, data to be analyzed is bounded by two process horizons: Tools Horizon and Analysis Horizons. Commonality of impacted lots in these horizons aims to highlight the tool most likely to be the source of defect. A prototype has been developed for the defectivity workshop in St-microelectronics in France and is used for the process diagnosis.
This paper is structured as follows. Section 2 describes the problem and lists the desirable characteristics of the diagnosis method. Section 3 reviews the diagnosis methods developed in semiconductor manufacturing industries and discusses their limitation. Section 4 shows how the diagnosis can be rapid and efficient. Section 5 discusses the result of the prototype test comparing to the existing method and section 6 concludes the paper with recommendations for further researches.

2. PROBLEM STATEMENT

To ensure the performance of the tools as well as the process line, two sampling strategies of lots are used: The first one is the Start Sampling Strategy where lots are selected at the beginning of the process and will be controlled following the control plan until the end of the manufacturing line. The second one is the smart sampling

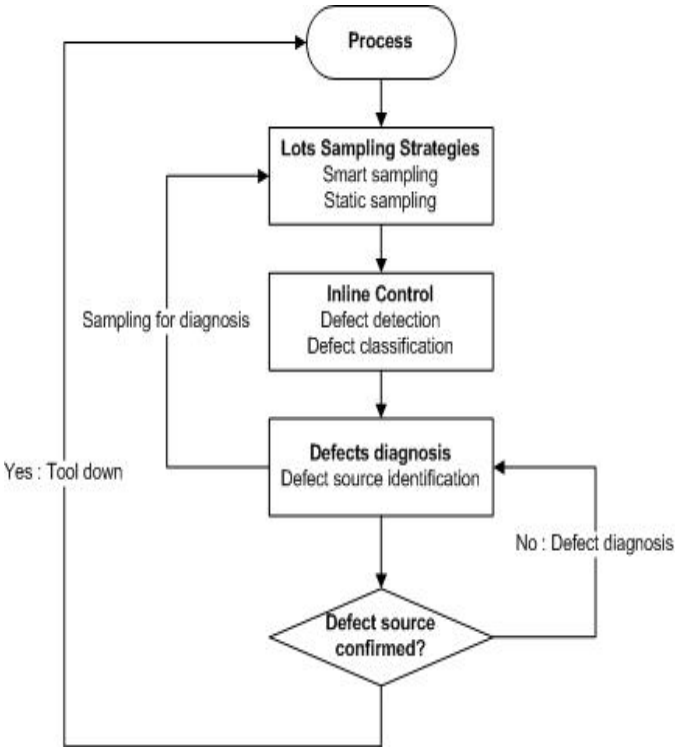

Fig. 2. Inline process monitoring

strategy which has been introduced to the system in order to reduce the number of controlled lots without any impact on the tools monitoring. See Dauzère-Pérès et al. [2010]. Since control step does not detect all the defects, a set of covered tools is defined for each control step throughout the control plan to guarantee all defects detection.
During the control, lots are classified as impacted or non-impacted lots. Whenever an impacted lot is detected, engineers are required to identify the defects source. Based on their business knowledge, engineers identify a list of suspected tools. Analysis of the historic process data of these tools aims to select similar lots for the control in order to confirm or reject the analyzed tools. This task will be repeated for all suspected tools which will increase the analysis time to more than seven days in some cases. An overview of the inline process monitoring is illustrated in Fig. 2.
Identification of defects source while the plant is still operating can help avoid more impacted lots and reduce productivity loss. Furthermore, a set of desirable characteristics of the diagnostic system is presented in the following.

2.1 Quick analysis

Reducing analysis time is challenging for the industries in order to quickly stop producing impacted lots. To prove the impact of analysis time on the number of impacted lots, we define:
TC: The time for lot to arrive to control step.
TA: The analysis time to identify defects source.
THn: The throughput of *tooln*.
The lots processed by *tooln* after the impacted lot are most probably impacted. The number of these lots is calculated as follows:

$$Numberoflots = \frac{TC + TA}{THn} \quad (1)$$

TC and THn are process dependent variables that are not modifiable. According to (1), the number of lots processed during an abnormal event in the process depends to the analysis time TA.

2.2 Identification of multiple defects source

The ability to identify multiple defects sources is an important but a difficult requirement for industries that are characterized by the re-entrant flow of the process. Defects diagnosis is more complex in such industries when the defects are generated by a combination of tools.

2.3 Classification error estimation

The defect diagnosis of impacted lots takes into account the defects classes. A misclassification of multiple defects classes on the same impacted lot causes a false diagnosis result.

2.4 Adaptability

More than two hundred products can be concurrently run in semiconductor plants. Process operating conditions can change due to changing the product and also production quantities. The process diagnosis should be adaptable to changes and able to identify the defect source of different products.

2.5 Data Extraction

In worldwide industries, process data are collected every day and stored in several databases. Therefore, two factors need to be considered by the process diagnosis method: First, the huge amount of data that has a direct impact on the extraction time. Second, the different format of data that has to be analyzed differently.
The challenge in our work is to develop a diagnosis method respecting the desirable characteristics in order to quickly identify the defects source and to stop producing impacted lots.

3. LITERATURE REVIEW

Tool Commonality Analysis (TCA) is believed to be an effective approach to identify defects source for yield diagnosis. Many successful applications of TCA has been reported in Langford et al. [2000] and Malinaric et al. [2000].
The formal term of TCA for semiconductor manufacturing yield diagnosis is first proposed by Kong [2002] where the author discusses and summarizes the critical elements of successful TCA, including sample size selection, raw data classification, statistical analysis, time series and analysis of tools with multiple entry points within the same process flow. Various researches of defects source identification based on TCA have been reported in Chen and Fan [2012], Kupp et al. [2011], and Hsu et al. [2012].
TCA methodologies apply statistical methods to compare the behaviors of each tool during the process of impacted and non-impacted lots and highlights the tool having different behavior during the process. The efficiency of these methods requires a large population of control data which is not found in case of defectivity control since smart sampling strategies are applied to select lots for inspection. When the defects on the wafer produces spatial patterns, it is usually a clue for the identification of defect source. Therefore, defect pattern recognition was the main topic of many studies during these last twenty years in semiconductor fabrication. Chen and Liu [2000] use the neural-network approach to recognize defect spatial pattern. Yuan and Kuo [2008] use a model-based clustering via Bayesian inference for detecting defect patterns. Li and Huang [2009] used a hybrid approach that integrates the Self-Organizing Map and Support Vector Machine while Ooi et al. [2013] generate in their system the Alternating Decision Tree (ADTree) that achieve pattern recognition. These methods provide information about the defect but do not indicate how to identify the source of these defects. Close to our study, authors in Shindo et al. [1997] and Shindo et al. [1999] propose a methodology for identifying the source of defects using defect type Pareto. By grouping a class of defect with the killer class, their result show that it is possible to guess the potential source of the excursion and prioritize the problem fixing procedure. Pepper et al. [2005] propose a classification scheme based on the optical attributes of inline, low resolution images in order to separate killer defects from non-killer ones. This allows lots to be automatically flagged and accelerated for further analysis. Munga et al. [2011] used the indicators of the smart sampling to provide in real time the number of lots potentially impacted in order to minimize yield losses.
In this paper, we draw our inspiration from these previous research works to develop a real time diagnosis system based on inline defectivity control.

4. APPROACH OVERVIEW

Terabytes of process data are collected every day and stored for the process analysis. Thus, analysis data should be bounded in order to reduce the diagnosis time. At this end, two horizons are defined: the first one is the set of tools to be analyzed and the second one is the manufacturing period of each tool to be analyzed. Process data and control data of the selected tools are collected from several databases. Studying the lots and the control data allow identifying more impacted lots that are similar in term of process. Intersection of the sets of tools that processed these impacted lots provide the set of suspected tools while intersection of the sets of process chambers that processed the impacted wafers provide the set of suspected chambers. The chart of Fig. 3 illustrates the algorithm of the proposed approach.

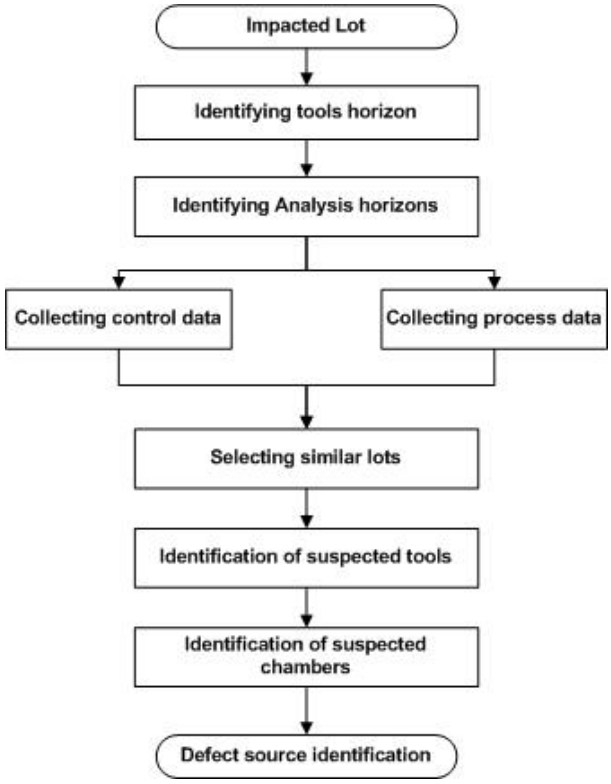

Fig. 3. Diagnosis approach of an impacted lot

4.1 Methodology Description

Tools horizon TH is the set of tools to be analyzed while analyses horizon AH is a tool-specific horizon defined as the manufacturing period of the process to be analyzed. To explain the tools horizon, we use the example illustrated in Fig. 4. Only $tool1$, $tool2$, and $tool3$ are covered by the defectivity control step, thus defects detected on lot $L1$ are made by one of these three tools where $TH = \{tool1, tool2, tool3\}$.

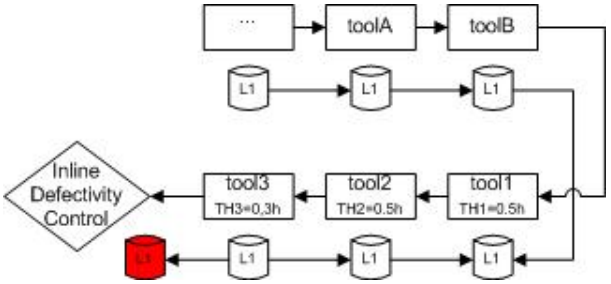

Fig. 4. Process flow of the impacted lot $L1$

Based on this example, we introduce the activities of tools in Fig. 5 to explain the analysis horizons. Each tool has its own limit and its own counter. Lots LA and LE are selected by the counter of $tool1$ while LF and $L1$ are selected by the counter of $tool2$ and lots LN and LB are selected by the counter $tool3$ for the defectivity control. Impacted lots are in red, non-impacted lots are in gray while lots in white are not controlled. Each tool in TH

Tool 1 (limit = 4)	
Lot	Counter
LA	4
LM	1
L1	2
LD	3
LE	4

Tool 2 (limit = 4)	
Lot	Counter
LM	3
LF	4
LC	1
LO	2
LN	3
L1	4

Tool 3 (limit = 5)	
Lot	Counter
LN	5
LO	1
LM	2
LC	3
LF	4
LB	5
L1	1

Control step
LA
LE
LF
LB
LN
L1

Fig. 5. Process tools activities and control

could be the source of defects. Thus, AH of $tooli$ is defined as the interval between the process time of the last non-impacted lot on the $tooli$ and the process time of the first impacted one.
In the analysis case of $tool1$, lot LA is classified as non-impacted lot in the defectivity control. LA is the last non-impacted lot before $L1$, it means that $tool1$ is not generating defects during the process of LA. Thus, AH^{tool1} is the interval time between LA and $L1$. LF selected by the counter of $tool2$ is classified non-impacted in the control step while $L1$ and LN are classified as impacted lots. AH^{tool2} is the interval time between LF and $L1$. $tool3$ processed the non-impacted lot LB before $L1$. Therefore, AH^{tool3} is the interval time between LB and $L1$.
Lots processed in these analysis horizons in this example are LM,LC,LO,LN,LF,LB, and $L1$. Synchronizing these lots with the control data provides a list of impacted lots that are similar to $L1$.
In the given example, the set of impacted lots contain now two lots: $L1$ and LN. LN has not been processed on $tool1$ while it has been processed before $L1$ in the analysis horizon of $tool2$ and it has been processed out of analysis horizon of $tool3$. Noting that on $tool3$, two non-impacted lots LB and LF are processed after LN and before $L1$. Therefore, $tool1$ and $tool3$ are removed from the set of suspected tools and $tool2$ that processed LN and $L1$ in the same analysis horizon, is the tool that generated defects.
To generalize the above interpretation, the following notations are introduced:
La: Lot to be analyzed.
LIM: Set of impacted lots.
$LIMH$: Set of impacted lots in the analyzed horizons.
$TSUS$: Set of suspected tools.
$T(Li)$: Set of tools processed the lot Li.
TH: Tools horizon.
AH^{Tj}: Analysis horizon of tool Tj.
$TCOV(D0)$: Set of covered tools of the defectivity control step $D0$.
$tLNL^{Tj}$: Process time of last non-impacted lot of production tool Tj.
$tLIL^{Tj}$: Process time of last impacted lot of production tool Tj.
$tTj(Li)$: Process time of lot Li on the tool Tj.
The analysis begin whenever an impacted lot La is detected at control step $D0$. Covered tools set defined for this control step represents the tools set to be analyzed (Tools Horizon).

$$TH = TCOV(D0) \tag{2}$$

The analysis time is impacted by the amount of data needed for the defect source identification. This data is proportional to the number of tools in TH. Thus, the number of tools to be analyzed has an impact on both analysis time and defect source identification.

Thanks to the smart sampling, performance of tools is guaranteed by a systematic sampling of lots on each tool for the control. Controlled lots (last non-impacted lot and last impacted lot) enclose the analyses horizon of tools as follows:

$$AH^{tj} =]tLNL^{Tj}; tLIL^{Tj}] / \forall Tj \in TH \tag{3}$$

Degradation time of each tool belongs to the Analysis horizon defined in (3). Therefore, the tools horizon and the analysis horizon allow look up for similar lots processed in the same context as the lot La. These lots are examined in order to select more impacted lots for the analysis.

$$LIMH = \{Li \mid \forall Li \in LIM \wedge t^{Tj}(Li) \in AH^{Tj}\} \tag{4}$$

The set of lots identified in (4) brings the impacted lots that are not only measured in a control step covering the tools of TH, but also processed during the analysis period of these tools.
The source of defects is common between all the impacted lots that are processed in the analysis horizon. Thus, suspected tools are given by the intersection of different sets of tools that processed lots in $LIMH$.

$$TSUS = \{\bigcap T(Li) \mid \forall Li \in LIMH\} \tag{5}$$

Set of suspected tools $TSUS$ in (5) depends to two variables: The first one is the number of lots in $LIMH$ and the second one is the set of process tools of each one. Therefore, increasing the number of lots in $LIMH$ decreases the number of tools in $TSUS$. If $TSUS$ contains only one tool, the source of defects is identified and the tool is turned down for the maintenance. In other cases, an advanced analysis of impacted wafers is useful to highlight for the suspected tools, the chambers to be checked.

4.2 Advanced analysis

Cluster tools are special integrated tools where several wafers can be processed in different chambers simultaneously. Analyzing the impacted wafers of lots provides the

set of suspected chambers of the tools. If the impacted wafers are processed in the same chamber, this chamber will be classified as suspected chamber.
To formalize this analysis, we introduce the following notions:
$WIM(Li)$: The set of impacted wafers of lot Li.
$WTIM$: The total set of impacted wafers.
$CH^{Tj}(WTIM)$: The chambers of tool Tj where the set of wafers $WTIM$ are processed.
SCH: The set of suspected chambers.
Identifying the suspected chambers requires at first the selection of impacted wafers. At this end, the set of lots identified in (4) is used as follows:

$$WTIM = \{\bigcup WIM(Li) \mid \forall Li \in LIMH\} \quad (6)$$

The set of wafers in (6) and the set of suspected tools in (5) are used to identify which elements have processed only the impacted wafers.

$$SCH = \{\bigcap CH^{Tj}(WTIM) \mid \forall Tj \in TSUS\} \quad (7)$$

Cluster tools have not the same number of process chambers. Therefore, the distribution of 25 wafers in a tool of "N" process chambers is different from a tool of "M" process chambers. In almost all cases, whenever a part of wafers in a lot are impacted, analysis identifies a unique suspected chamber. However, no suspected chamber can be identified in case all wafers of the lot are impacted.

5. INDUSTRIAL APPLICATION

A prototype has been developed in order to test the proposed approach on real data in ST microelectronics. Based on the control data and the process data, the prototype automatizes the analysis in order to display a list of suspected tools and suspected chambers. The behavior information of the tools such as alarms and maintenance interventions could be displayed as option.
The algorithm was run in parallel with existing method using the same data on different analysis examples. To evaluate the result, we highlight three indicators which are: the number of controlled lots, the number of suspected tools and the analysis time in minutes.
Based on their business knowledge, engineers extract the data to be analyzed in excel files for the manual analysis while the automatic algorithm allow extracting larger amount of data in less time. Realized tests are classified depending on their number of controlled lots into three categories (input) while the analysis time and the number of identified tools (output) are collected for both methods. Table 1 shows that the proposed method is more efficient than the existing one in time analysis as well as in suspected tools identification. Using the previous method, analysis time required between 60 and 180 mins in order to identify the suspected tools. While using the new one, analysis time is reduced for all the studied cases which now require not more than 5 to 10 mins, which means economizing more than 60% of working cost. This is due to the effectiveness of analyzing data identification in (2) and (3).
In the first case studies where there are more than four controlled lots, one suspected tool has been identified by both methods. While in the second case studies where

% from total cases	*Number of controlled lots(NL)*	*Analysis time (mins)*	*Number of suspected tools(NT)*
50 %	*NL > 4*	*Existing method*	
		60 ≤ t ≤ 90	*NT = 1*
		Prototype method	
		5 ≤ t ≤ 10	*NT = 1*
35 %	*2 ≤ NL ≤ 4*	*Existing method*	
		90 ≤ t ≤ 120	*2 ≤ NT ≤ 5*
		Prototype	
		5≤ t ≤ 10	*1 ≤ NT ≤ 3*
15 %	*NL = 1*	*Existing method*	
		90 ≤ t ≤ 180	*NT ≥ 5*
		Prototype method	
		5≤ t ≤ 10	*3 ≤ NT ≤5*

Table 1. Comparison Table

there are from two to four controlled lots, this new method helps decreasing the number of suspected tools to less than three instead of five.This reduction is mainly due to the advanced analysis of impacted wafers shown in (7). However, in the third case studies where the impacted lot is unique, both methods did not succeed into finding one suspected tool. Even though, the new one has reduced the number of suspected tools from more than five til three to five suspects.
The remarkable feature is the correlation between number of impacted lots and the suspected tools as demonstrated in (5). The more affected lots are available the less suspected tools are identified. Affected lots which are processed in the same analysis horizons are similar in term of production tools and process time.

6. DISCUSSION AND CONCLUSION

Real time process diagnosis for semiconductor manufacturing line is described in this paper. Tools horizons and analysis horizons are defined in order to identify the data to be analyzed. Based on defectivity control, analyzing the impacted lots aims to identify the set of suspected tools and analyzing the impacted wafers highlights the chambers that are most likely the source of defects.
A prototype has been developed and result shows a correlation between the number of impacted lots and the number of suspected tools. This brings to our attention the need for a sampling algorithm that takes into account the degree of similarity of lots. Using such an algorithm, classification of lots will be performed in order to select lots from the same class to be measured. For this purpose, future work will be dedicated to two researches axes:

(1) Classification of lots based on the process steps alignment using T-Coffee method presented in Notredame

et al. [2000]. This method has been used successfully to align process plans in semiconductor applications by Viale et al. [2011].

(2) Calculating of decision support indicator for each suspected tool using the collected information such as alarms and maintenance interventions.

The re-entrant flow of the process and the cluster tools used in semiconductor manufacturing line allow using the commonality analysis for process diagnosis in two levels: Impacted lots analysis and impacted wafers analysis. This diagnosis approach can be used in other industries having at least one of the above characteristics.

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