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Inter power electronic building blocks' communication over two optical rings

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Abstract: Power electronic building blocks, initiated and sponsored by the Office of Naval Research, are based on the integration of power semiconductor elements with some degree of intelligence and data communication capability in compact form. This article addresses the communication issues between power electronic building blocks. A study case of Inter PEBB communication is described, based on two-optical ring topology and the possibility of complete implementation in a single FPGA for slave nodes.

Keywords: power electronic building block, communication, FPGA

1. INTRODUCTION

The concept of the power electronic building block (PEBB), initiated by the Office of Naval Research is based on the integration of power semiconductor elements, and some degree of intelligence for local control and data communication capabilities. This would enabling the possibility of (i) building a more complex power electronic device (PED) or power electronic system (PES) from PEBBs by simple linked PEBBs in a standardized way with a power supply bus and inter-PEBB communication (IPC) system, and (ii) by a software determination of the built device function.

This concept is heavily dependent on standardization, which should ensure a prior guarantee of mutual compatibility regarding each of the four PEBB's interfaces (Fig. 1) at each PEBB power level. In addition, the concept

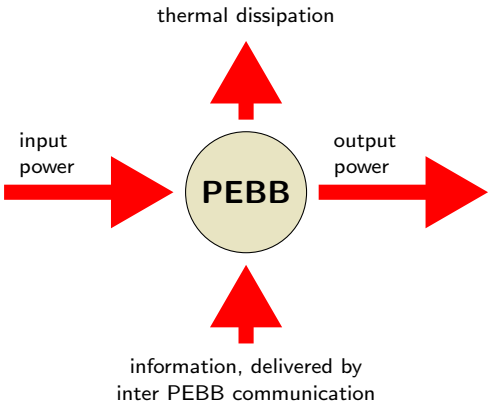

Fig. 1. PEBB module interfaces.

of building PED or PES from PEBBs with distributed control linked by inter-PEBB communication, needed to be well-understood, see Boroyevich [1995], Milosavljevic [1999], Cucej [2001, 2003], Francis [2006].

The recent development of fast semiconductor switches and converters' topologies shows that, in the near future medium power PEBBs will cross at a class higher switching frequency. This means that a digital controller for medium power PED/PES – which today already crosses at switching frequency of over 100 kHz – should be capables of performing control tasks at 10 μs sample intervals (Fig. 2).

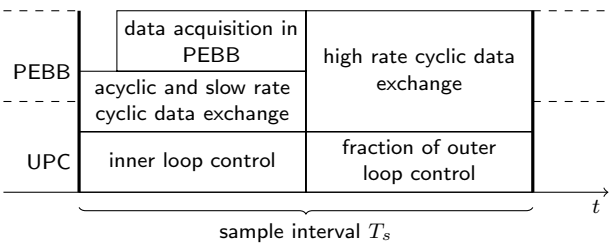

Fig. 2. Sample interval sharing between inner control algorithm, data acquisition, and cyclical data communication. The outer control algorithm can be distributed over a number of cyclical data communication intervals.

The control of object or process feeded by PED/PES consisting of PEBBs is typically a cascade structure, where the outer-loop is dedicated to object control and the inner-loop to PED/PES control. Fortunately – from the points of control as well as IPC – there can be a significant difference between the outer-loop control intervals and the sampling interval used in inner-loop of the controller. Consequently, the IPC must provide only a share of data used in the outer-loop and, of course, all the data for the inner-loop (Fig. 2).

2. INTER PEBB COMMUNICATION

Requirements for IPC are:

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(1) deterministic,
(2) being already immune to the disturbance, crosstalk, and interference as much as possible on the physical level,
(3) capable of allowing the diverse IPC traffic needed for normal PEBB functioning, support reconfiguration of PEBB, monitoring of PEBB states by boundary scan, etc,
(4) reliable, scalable, and survivable.

Analysis of existing fieldbuses, see Milosavljevic [1999], showed that the features of MACRO, see Delta-Tau Data Systems [1998], lie closest to the above enumerated requirements. No wonder it was selected for the "first generation" of IPCs.

A concise description of the functions of IPC are offered by the IPC reference model (Fig. 3). This model's layers

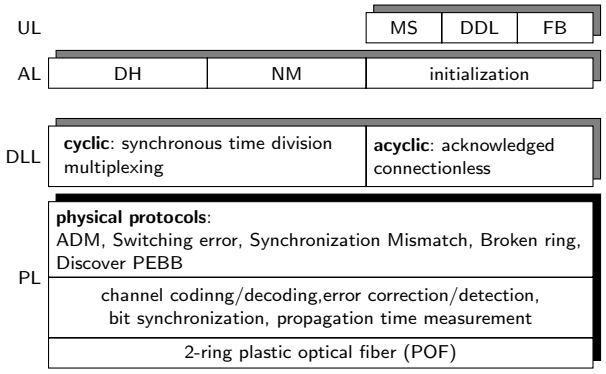


Fig. 3. IPC reference model. Legend:
MS: Message Specification. The IPC equivalent to Fieldbus Message Specification (FMS) of variables.
DDL: Device Description Language, serves for description of the HML function.
FB: Function Blocks.
DH: Data Handler. Its function is data mapping from IPC into Intra PEBB communication, exchange data with smart sensors or with application in UPC.
NM: Network Management.
UL: User Layer, AL: Application Layer, DLL: Data Link Layer, PL: Physical Layer.

from UL to DLL are implemented only in master node in UBC. Implementation of a physical layer function in the master node has minor differences from implementation in the slave nodes.

3. A CASE STUDY

The starting point of the case study was an existing IPC based on MACRO protocol, see Cucej [2003], and later considered achievements presented by Francis [2006]. The *master/slave* concept with one master was preserved from MACRO. The physical layer was enriched with the second optical ring using a traffic direction opposite to the direction in the first ring (Fig. 4). The function of TAXI chips with the latter described extensions was implemented in FPGA (consequently achieved data rate on one ring due to speed limitation of used FPGA was reduced to 25 Mbit/s). A new synchronizer was developed, as well as a function for topology reconfiguration. Besides this the new frame

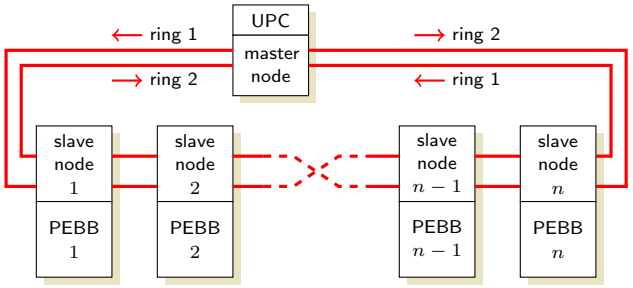


Fig. 4. IPC with two active optical ring topology.

organization, forward error coding scheme, and the simplification of those protocols implemented in slave node, i.e. in a PEBB, were tested.

When using two-optical ring topology, the price of physical transmission is doubled in comparison with one ring topology. However, two-ring topology with opposite data flow is far more reliable and survivable as one-ring topology and also enables relatively simple protocol-independent local synchronization of sampling instants. Furthermore, the transmission capacity is doubled, when using two rings. This can be exploited in different ways, for example, by doubling the maximal number of PEBBs, or halving the sampling interval and, thus, doubling the total switching frequency of PED/PES or halving the one-ring IPC bit rate.

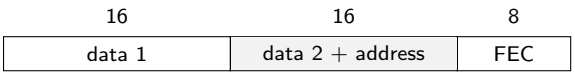
From the aforementioned possibilities, the following were considered in the case study:

- reconfiguration of two-ring topology over one sample interval,
- doubling the number of PEBBs in an IPC,
- locally performed synchronization, which is based on measurements of the frames' propagation times.

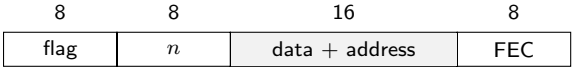
Besides the aforementioned, the structures of all frames were revised for better utilization of sampling intervals.

3.1 Frames

Information frames (Fig. 5a), in short I-frames, contain two 16-bit long slots, which enable UPC to send two words of switch on/off occurrence data and, at the same time, to collect the same amount of fast changing measured data in PEBB. Two slots follow FEC which contain BHC (Bose-Chodhuri-Hasquenghen) code with generator polynomial $x^8 + x^2 + x + 1$, the same as used in ATM, see Stalings [1996]. Since a FEC protects only 32 data bits, it creates enough redundance for correcting 1-bit error and discovering any 2-bit error and 8-bit burst error.



(a) data frame



(b) supervise frames

Fig. 5. Formats of frames (before 4B/5B encoding).

The second slot also contains the address of PEBB, which is superimposed onto the data. This additional PEBB address serves many purposes, as described later. The slave nodes check if the data really belongs to it, in the following way:

(1) from the received data subtract own address
(2) calculate the FEC
(3) if none or only one-bit error is discovered, the received, the data is intended for this node. If the burst of the least two-bit error is discovered, the frame is not copied into PEBB and the *synchronization mismatch* frame is generated.

The condition for the proper work of the aforementioned is obvious – the Hamming distance between any pair of addresses should be larger than three.

Supervise frames (Fig. 5b), in short S-frames, have the same size as I-frames. Instead of the first data slot they have an 8-bit long flag with repeated 4-bit code with a type of S-frame, Table 1. The 8-bit field is followed by the number of I-frames.

Table 1. S-frames.

from UPC to PEBB	from PEBB to UPC
Start of Convoy	Switching Error
Sample Instant Synchronization	Synchronization Mismatch
Master Reset	Broken Ring
Initialization	
Discover node	
Acknowledge	

During the cyclical data exchange, the data frames are sent in a convoy consisting of S-frame *Start of Convoy* as head of convoy followed by I-frames in opposite order to what they are as PEBBs in the traffic direction and, finally, S-frame *Sample Instant Synchronization* as a trailer. The gap between the trailer and the end of sample interval is padded with padding bits (Fig. 6).

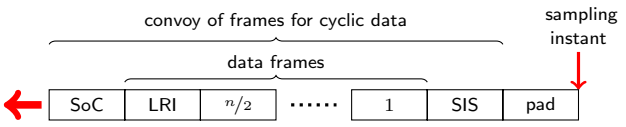


Fig. 6. Structure of convoy. SoC: S-frame *Start of Convoy*, LRI: low rate I-frame, SIS: *Sample Instant Synchronization*, pad: padding bits. The data frame numbers are equal to the positions of slave nodes in the direction of the convoy propagation down the optical ring.

3.2 Transceiver circuit

The transceiver circuit in the slave nodes (Fig. 7), enables wire speed detection of S-frames. Since the data frames travel in convoy with the SoC frame as header and the SIS frame as trailer, it is easy to determine those time slots in which PEBB's nodes copy data into the receiver shift register, and simultaneously replace this data with their own. Slots are determined by the cyclical data frame counter and slot decoder, which is configured during the initialization phase using the S-frame *Discover node*.

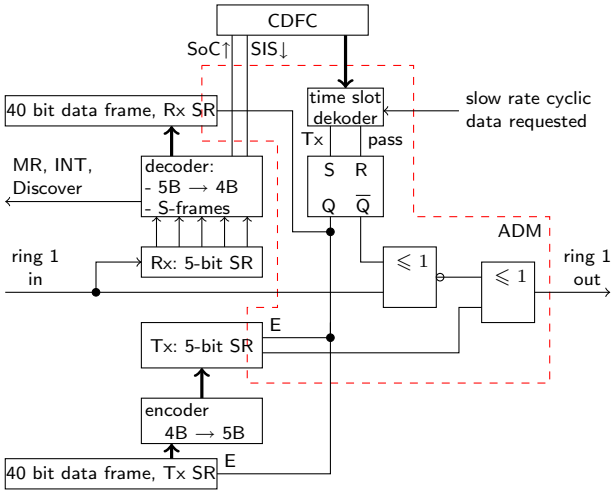


Fig. 7. Principle of an innovative transceiver circuit in the first ring. CDFC: Cyclic Data Frame Counter, ADM: Add Drop-away Multiplexer.

Any delay in the data streams in one node is caused by delays of the optical receiver and transmitter, as well as delays by successive inverters serving for ADM time consistency (as with many other details, it isn't shown in the figure), and delay of ADM.

3.3 Exchanges of fast rate cyclical data

The exchanges of fast rate cyclical data are performed by ADM (Fig. 7) at wire-speed. In the PEBB's node, fast-rate cyclical data are stored in a 32-bits shift register (SR). During transmission FEC is calculated on-the-fly and added at the end of the sent data. 4B/5B encoding is performed in steps of 4-bit data sequences, also on-the-fly.

3.4 Collection of slow rate cyclical data

The slow rate data are stored in PEBB's node, in a special buffer. Pulling data from the buffer activates acquisition of this data in PEBB.

The collection of slow-rate cyclical data from PEBB's node is controlled by a master node in UPC. It selects the node by putting the node address into the SoC frame data field. When a node in SoC detects its own address, it sets up a signal *slow rate cyclical data requested*. Then, in the same way as for fast-rate cyclical data, it replaces the content in the LRI frame, using the prepared data.

3.5 Acyclic traffic

Acyclic traffic is used on two occasions:

(1) during the initialization phase,
(2) when an irregular event happens in PEBB.

During the initialization phase, the traffic is initiated and controlled in a master/slave fashion by UPC. Among the S-frames used for initialization are *master reset*, *Initialization*, *Discover node*, *Acknowledge* and *Sample Instant Synchronization*. The procedure is described later.

When collecting irregular events, UPC in the sample subinterval intended for acyclic traffic, successively sends

empty frames *Switching Error* (SE) and *Synchronization Mismatch* (SM). These frames in the data field carry a set of 16 flags, each assigned to one PEBB. If the PEBB experiences this failure, PEBB's nodes set-up an assigned flag to it. If there are more than 16 PEBBs connected within one ring, they are segmented into groups of 16 PEBBs and the groups are assigned within the field n.

A broken ring is signalled by S-frame *Broken Ring* (BR) on the second ring, immediately after detecting ring breakdown. Apparently, the broken ring is detected successively in all nodes after failure (in the second ring direction) on the ring. For resolving possible collision and for detecting the place of failure, BR frames are sent successively as long as that slave nodes from the master node receive:

- ACK frame with instructions/confirmation for reconfiguration two-ring network into two one-ring networks, or
- MR frame with request to shutdown the PEBB (all switches go to the off-state)

A collision arises if the next node detects a broken ring before it detects the arrival of a BR frame from a node closer to failure. In this case the signal *alert ring broken* in nodes activates sending their BR frames, which is discontinued by detection of the incoming BR frame. With detection of an incoming BR frame, the flag *ring is broken before previous node*, is set. This flag after momentarily sending a BR frame heading, prevents any further sending from this node (Fig. 8). Consequently, the master node

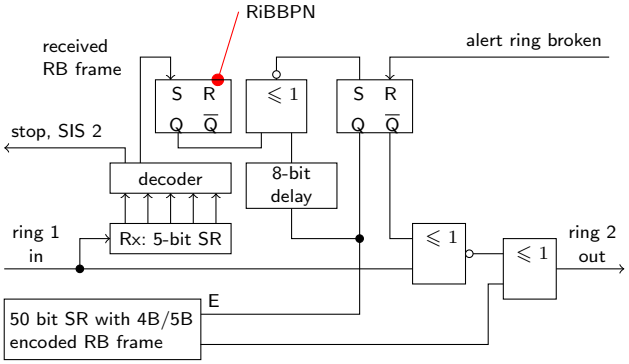


Fig. 8. Block scheme of transceiver circuit parts in the second ring involved in physical protocol "Broken Ring". RiBBPN: flag "Ring is Broken Before Previous Node", SR: Shift Register, E: enable.

reach at least one complete BR frame header which, on its way to the master node set in the all passed slave nodes, flags *ring is broken before previous node*. This procedure cleans-up the ring for the the BR frame from node which is closest to the ring failure.

3.6 Synchronization

The purpose of synchronization is for determining and maintaining sampling instants' synchronization in each PEBB. Synchronization is based on the measurement of time difference between SIS frame recognition instant in frame convoys which are simultaneously transmitted, each on its own ring. Since convoys propagate in opposite directions down the ring, both SIS frames pass each other close to midway. At this point the time difference between them is zero. At each other slave node this difference is twice the offset gap between the SIS frame recognition instant, and the sampling instant. This gap is padded with padding bits (Fig. 6).

Synchronization is performed by two counters, one buffer, a comparator, and two pre-scaler counters (Fig. 9). Counter 1 serves for determining the gap between the occurrence of synchronization frame detection and sampling instant, the second counter serves for measuring frame propagation time. It has a complex structure, because, for the sake of generality, it can determine half and full differences between both frames' convoys, and also supervise if a ring is broken. The measured difference is stored in a buffer since it is used for the next sampling interval. The buffer also stores data from this SIS frame, which determines ratio *VCO clock/bit rate* ($\times 2, \times 4, \times 8, \times 16$) and the ratio between the measured time difference of SIS frames, and the gap to sampling instant (can be 1:1 or 2:1).

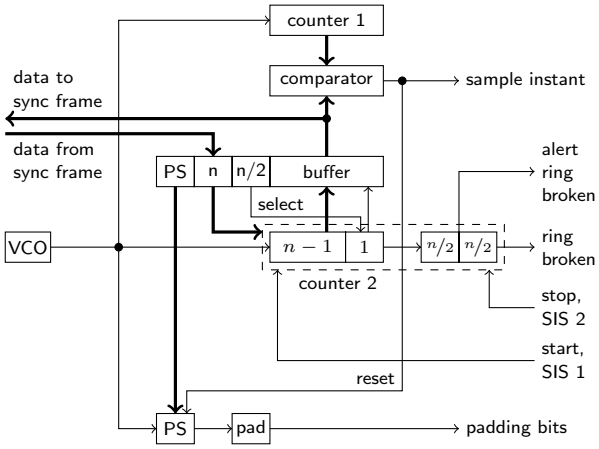


Fig. 9. Scheme of synchronizer. For meaning of label see text below.

Blocks "pad" and pre-scaler PS_2 serves for adjusting padding bits. When resetting PS_2 the first padding bit width is adjusted such that any jitter of sampling instants is minimized. The amount of jitter depends on the accuracy of the difference measurement, i.e. from ratio *VCO clock/bit rate*. If this ratio is 2:1, then the jitter is less than $\pm 0.05\,\%$, in the case of 16:1 it is improved to $\pm 0.006\,\%$. Since only the length of the first padding bit in the sample interval can vary, only slightly disturb not disturb the bit synchronization.

The described synchronization considers the propagation of signals along the transmission media too. This becomes important when the PEBBs are spread around and length of transmission media between them can not be neglected anymore.

3.7 Initialization

Initialization has two parts:

(1) initialization of PEBB
(2) auto-configuration of communication system

Slave nodes support the executing PED/PES initialization by delivering the received initialization data into the

PEBB control registers, reading status registers, and supporting the acknowledged connectionless services of the acyclic data transfer. Frames received without errors or with one error corrected by FEC, are acknowledged by the ACK frame in a packet of up to 16 data frames, following the initialization frame.

Under normal circumstances the IPC is set-up during the design of PED/PES. For the sake of reliability at the fault tolerant design of PED/PES, the PEBB's nodes support reconfiguration, in the case of ring break as described in section 3.5, as well as the auto-configuration of IPC at the initialization of the communication system.

The main goals for the auto-configurations of PEBB's nodes are determining the nodes' serial order in the optical ring. This procedure has two steps. In the first step, the master node in the UPC sends S-frame "Discover node", which activates the automaton for setting-up the decoder for read or setting the flags in the S-frames (in accordance with a node place in the ring), in the second step the master node successively sends the logical addresses of the nodes by frame pairs 'Discover node" and I-frame. In the S-frame's data field node is assigned by its place in the ring, and in the followed data frame the data slots contain the nodes' logical addresses, determined by the master node.

4. CONCLUSIONS

IPC is not only a challenge for PED/PES consisting of PEBBs, but is highly attractive for classically designed converters of any kind too. Its benefits are higher reliability, simpler installation and, consequently, lower maintenance costs. These make it, regardless of higher starting costs, a very competitive solution in comparison with the existing wired-system, especially together with the described UPC, when it is used in medium and high power inverters or converters.

IPC is very demanding at function execution times, consequently communication protocols have to be executed at so-called wire-speed at a bit rate of a least 100 Mbit/s. Therefore, all function are simplified as much as possible. For example, all protocols in the slave node are physical protocols realized by automaton, logic and counters, and implemented in FPGA.

Two-ring topology compensates for the double cost of transmission media and the necessary electro-optical couplers with high value benefits such as:

- enabling independent self synchronization in each node on IPC
- higher reliability and survivability of PED/PES

From the performed simulations in VHDL and the implemented parts of IPC in FPGA, we experienced the fact, that today FPGA enables the building-up of compact IPC master node as well slave nodes with integrated HML functions, in a single chip solution.

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