Proceedings of the 17th World Congress
The International Federation of Automatic Control
Seoul, Korea, July 6-11, 2008

LOW-COST EMBEDDED SOLUTION FOR MEASURING POWER QUALITY PARAMETERS

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Abstract: Power quality issues are becoming a serious concern for electrical power users considering the negative influence that these phenomena can have on the electrical equipment and the utility bill. That is why more solutions are required for measuring the power quality parameters. This paper presents a low-cost approach based on an inexpensive RISC microprocessor and frequency analysis for constant measuring and monitoring of specific parameters.

1. INTRODUCTION

In the last years the power quality problems have become increasingly interesting for the customers because of the negative effects on the electrical equipment. This leads to a greater demand for the power quality measurement tools and especially for the low-cost instruments.

Power quality is a term used to define any occurrence of voltage, current or frequency deviation that results in equipment failure, process interruptions or power system inefficiency. These deviations manifest themselves as harmonics, low power factor, voltage sags/swells, voltage flickering, transients and many other forms. The importance of measuring these phenomena comes from the undesired effects caused to the electrical equipment and utility bill.

Harmonic disturbances can cause several problems such as increasing losses, erroneous operation of protective devices, inaccurate power metering, equipment overheating, motor vibration, can cause disturbance to control systems and communicational systems and destroy the factory productions (Gready and Santoso, 2001).

Voltage sags, also known as voltage drops or under-voltages are caused by local loads, during either motor startup or rapidly changing loads. This condition is characterized by low power factor and high reactive energy demand.

In many cases, low power factor result in higher utility bills through penalties and increased demand charges. They also cause system energy losses, overheating, increased maintenance cost and low service utilization.

On the market are available high performance products for measuring power quality parameters but this approach leads to high costs and it is inappropriate for constant and continuous measurement and recording of the targeted parameters.

A different approach may be the usage of low-cost, low-power dedicated tools that could be specialized and constant monitories specific parameters.

2. POWER QUALITY DISTURBANCES

When talking about power quality is very important to have a correct description for the phenomena that can appear and an exact numerical characterisation for these events. This is why the definition and classification of these events from IEEE Std. 1152 provides a useful starting-point for a power quality analyzer tool.

The deviation from a perfect sine wave can be represented by harmonics, which are nothing but sinusoidal components having a frequency that is an integral multiple of the fundamental frequency. The harmonics amplitude is between 0-20% from the fundamental's amplitude.

Voltage sag is described as a drop of 10-90% of the rated system voltage lasting for half a cycle to 1 min.

Voltage swells are defined as the increase of fundamental frequency voltage for a short duration lasting for half a cycle to 1 min. The typical values are 110-180% of the rated system voltage.

The power factor of an AC electric power system is defined as the ratio of the real power to the apparent power where the real power is the capacity of the circuit for performing work in a particular time. Apparent power is the product of the current and voltage of the circuit. Due to energy stored in the

load and returned to the source or due to a non-linear load that distorts the wave shape of the current drawn from the source, the apparent power can be greater than the real power. Low-power-factor loads increase losses in a power distribution system and result in increased energy costs.

3. THE FAST FOURIER TRANSFORM

Expressing the signal in the z-transform and evaluating the spectrum on the unit circle can provide a frequency analysis of a digital signal. The discrete-time Fourier transform (DTFT) is defined as

$$X(\omega) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n} \tag{1}$$

The DTFT X(ω) is a function of a continuous-frequency variable ω, and summation (1) extends towards positive and negative infinity. Therefore the DTFT is a theoretical Fourier transform of a digital signal, but it cannot be implemented for real applications (Kuo, and Can, 2005).

Frequency analysis of a finite-length sequence, the discrete Fourier transform (DFT) is equal to the sampled version of the DTFT. In other words, the continuous-frequency variable ω is sampled at N equally spaced frequencies

$$\omega_k = \frac{2\pi k}{N} \tag{2}$$

k=0, 1…N-1 on the unit circle. These frequency samples (DFT coefficients) are expressed as

$$X(k) = X(\omega_k)\,|_{\omega_k = 2\pi k/N} = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}$$

$$= \sum_{n=0}^{N-1} x(n) W_N^{kn}, k = 0,1 \ldots N-1 \tag{3}$$

where the twiddle factors are defined as

$$W_N^{kn} = e^{-j(\frac{2\pi}{N})kn} = \cos(\frac{2\pi kn}{N}) - j\sin(\frac{2\pi kn}{N}) \tag{4}$$

The DFT is based on the assumption that the signal x(n) is periodic. Therefore, X(k) for k=0, 1, …, N-1 can uniquely represent a periodic sequence x(n) of period N.

To compute a complete set of N DFT coefficients, N×N complex multiplications and N×(N-1) complex additions are required, which can be simply stated as a complexity of order $O(N^2)$. This algorithm has a high computational load this is why more rapid computational schemes are required.

The Fast Fourier Transform (FFT) algorithms were first introduced in the field of digital signal processing by Cooley and Tukey (Cooley and Tukey, 1965). They used an divide and conquer algorithm that recursively breaks down a DFT of any composite size N = N1N2 into many smaller DFTs of sizes N1 and N2, along with O(N) multiplications by complex roots of unity called twiddle factors.

One of these algorithms is called decimation-in-frequency algorithm. To derive the data it begins by splitting the DFT formula in two summations, one which involves the sum over the first N/2 data points and the second sum involves the last N/2 data points. Thus is obtained

$$\mathrm{X(k)} = \sum_{n=0}^{(N/2)-1} x(n) W_N^{kn} + \sum_{n=N/2}^{N-1} x(n) W_N^{kn} \tag{5}$$

$$= \sum_{n=0}^{(N/2)-1} x(n) W_N^{kn} + \sum_{n=0}^{(N/2)-1} x(n+\frac{N}{2}) W_N^{kn} W_N^{(N/2)k}$$

Since $W_N^{(N/2)k} = (-1)^k$, the equation (5) can be simplified to

$$\mathrm{X(k)} = \sum_{n=0}^{(N/2)-1} \left[x(n) + (-1)^k x\left(n + \frac{N}{2}\right) \right] W_N^{kn} \tag{6}$$

This equation can be further expanded into two parts: one for even samples X(2k) and the other for odd samples X(2k+1). In addition the equation (6) can be partitioned as

$$\mathrm{X(2k)} = \sum_{n=0}^{(N/2)-1} \left[x(n) + x\left(n + \frac{N}{2}\right) \right] W_{N/2}^{kn}$$

$$= \sum_{n=0}^{(N/2)-1} x_1(n) W_{N/2}^{kn} \tag{7}$$

and

$$\mathrm{X(2k+1)} = \sum_{n=0}^{(N/2)-1} \left[x(n) - x\left(n + \frac{N}{2}\right) \right] W_N^n W_{N/2}^{kn}$$

$$= \sum_{n=0}^{(N/2)-1} x_2(n) W_N^n W_{N/2}^{kn} \tag{8}$$

for k=0,1, … (N/2)-1.

The computational procedure above can be repeated through decimation of the *N*/2-point DFTs *X*(2*k*) and *X*(2*k*+1). The entire process involves $v = \log_2 N$ stages of decimation, where each stage involves *N*/2 butterflies of the type shown in Fig. 1. Consequently, the computation of the N-point DFT via the decimation-in-frequency FFT requires (*N*/2) $\log_2$N complex multiplications and $N\log_2 N$ complex additions. (Kuo, and Can, 2005).

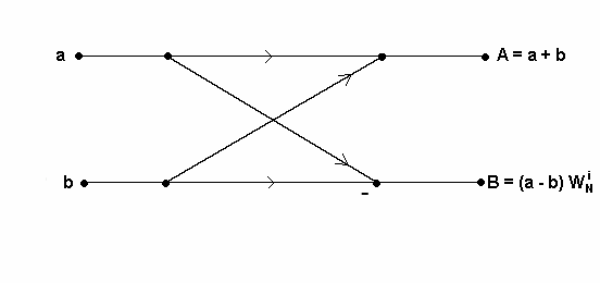

Fig. 1 Basic butterfly computation in the decimation-in-frequency

4. MSP430F1xx ULTRA-LOW POWER MICROCONTROLLERS

The Texas Instruments MSP430 family of ultra-low power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The MSP430x15x/16x/161x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, dual 12-bit D/A converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), I2C, DMA, and 48 I/O pins. Typical applications include sensor systems, industrial control applications, hand-held meters, etc. (Texas Instruments 2006).

The features that recommend the MSP430F1xx microcontrollers for the current application are: the 16-bit 8MIPS RISC CPU, the 12-bit A/D converter, the 3-channel DMA controller, the 16-bit built-in timer and the Hardware Multiplier.

The A/D converter with the 16-bit timer and the DMA controller can sample the analogue signal at an exact rate and save the obtained data into the memory without CPU intervention. This provides a very important advantage in terms of processing time, because the CPU can simultaneous effectuate the required computations on a complete set of data.

The Hardware Multiplier is also a very important peripheral because it can compute 16-bit signed multiplications in one cycle without CPU intervention, and has a 32-bit result register that can solve the overflow problem for the 16×16-bit multiplication.

The application's hardware is pictured in the Fig. 2 and is composed from:

a. Microcontroller MSP430F169

b. MSP430 Starter Kit that includes: MSP-FET430PIF (parallel JTAG debugging and programming interface) and the 64-pin target board

c. Test board for signal acquisition

d. LCD display

e. Computer for software development

f. Level shifter circuitry from 3V to RS-232

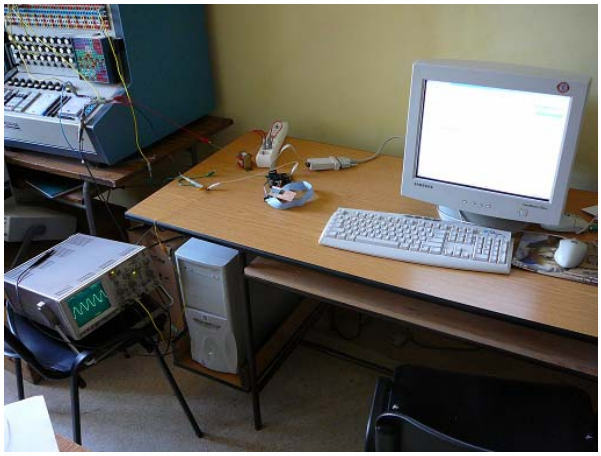

Fig. 2 Application hardware

A detailed view of the application is presented in Fig. 3 where are pictured only the MSP 430 target board, the parallel JTAG programming interface and the LCD display.

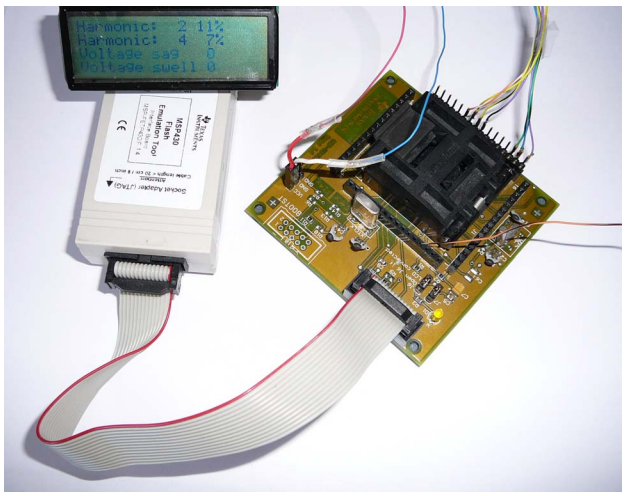

Fig. 3 Application hardware (detail)

5. SOFTWARE IMPLEMENTATION

For the software implementation of the low-cost power quality analyzer we chose to implement an classical 2-radix, division-in-frequency FFT algorithm with little modifications due to the limited hardware resources available (8 MIPS computational power and 16-bit architecture). The FFT was computed on two 128 samples arrays (one for voltage and one for current).

In the implementation we tried to maximize the benefits from using the microcontroller's peripherals and to minimize the

limitations imposed by the low-cost processor. The application structure is typical for signal processing domain.

The analogue input signal is sampled with an exact frequency by the A/D converter. A finished conversion triggers the DMA controller that moves the data in the input arrays from the memory. These operations take place without CPU intervention. When a full buffer is received a flag is set and the CPU moves the data in another buffer using the DMA controller and begins the data processing. When this is done the results are available to be displayed on the LCD or to be sent to a computer over the serial interface and the CPU can begin processing another buffer.

In order to communicate with a computer over the serial interface has been used a level shifter circuitry based on the MAX2322 chip, and one of the serial interfaces of the microprocessor. This is very useful in terms of analysing and verifying the results obtained with the microcontroller because we are able to send the input data and the results to a personal computer, to process the data in LabVIEW and compare the results. The communication over the serial interface can be very useful in the future because it enables the embedded application to communicate with a computer-based software opening new opportunities for control, data-logging, data-analyzing and data-displaying.

5.1 FFT Algorithm implementation

In order to reduce the computational overhead we pre-calculated the twiddle coefficients and stored them in 2 arrays. Additionally, because of the 16-bit RISC architecture these coefficients were normalised with a factor of 1024 and converted to integers. This way all the multiplications that involve the twiddle coefficients were made on the hardware multiplier, taking advantage on the 32-bit result register, and the result was re-scaled by dividing with 1024, resulting as operands only 16-bit integers.

When computing the complex multiplies from the butterfly scheme we used a scaling factor of 0.5 to avoid the 16-bit overflow.

We must note that due to hardware limitations (the A/D converter can convert only positive values) we were forced to introduce a DC offset in order to capture the sinusoidal waveform. This offset is then removed by software.

The sampling frequency was calculated according to the algorithm requirements and we used 6400 samples/second to analyze, with a 128 points FFT the signal from the power supply network that has the fundamental frequency at 50 Hz.

6. RESULTS

6.1 An experiment

The application has been used to analyze the voltage and current from a circuit that contained a capacitive load. For the sampled signal shown in Fig. 4 had been obtained, after applying the FFT, the results shown in Fig.5 (voltage) and Fig 6 (current). For illustration purposes only, the input data and the result were plotted using LabVIEW.

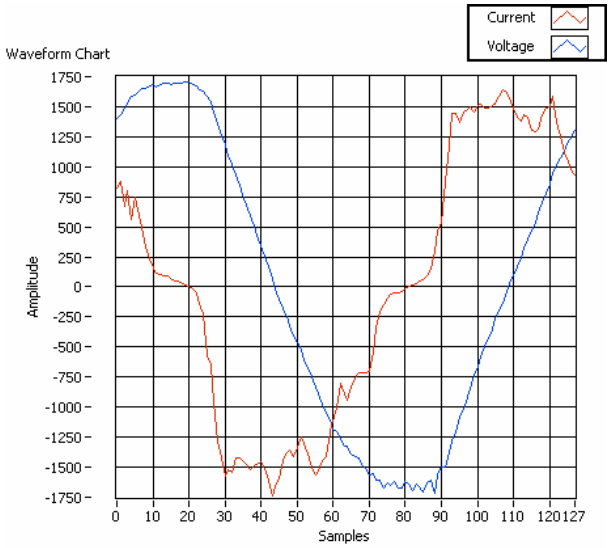

Fig. 4 Input data buffer

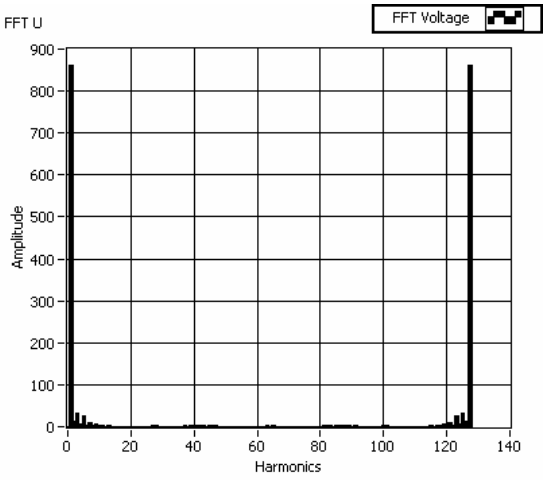

Fig. 5 FFT voltage

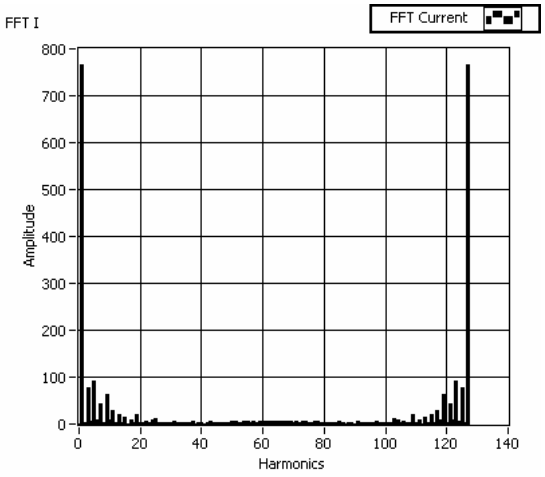

Fig. 6 FFT current

The results from the voltage FFT show a very high value for the 50 Hz fundamental and the 2nd and 4th harmonics distinguish themselves from the rest. The 4th harmonic has a numerical value that corresponds to 2.91% from the fundamental's value. The 2nd harmonic numerical value is equal with 3.76% from the fundamental's amplitude. We must note that the DC offset introduced due to hardware limitations of the A/D converter was removed by software.

In Table 1 are presented relevant numerical values from this experiment to compare the results obtained on the microcontroller with the reference values obtained in LabVIEW. We also computed the Relative Error with the formula:

$$\text{Re}l\_Err = \frac{reference\_val - calc\_val}{reference\_val} * 100 \quad (9)$$

Table 1. Experimental results FFT current

Parameter	MSP	LabVIEW	Relative Error (%)
Fundamental's Amplitude	768	98106	0.2
1st harmonic (%)	0.39	0.41	4.87
2nd harmonic (%)	9.5	9.72	2.31
3rd harmonic (%)	0.91	0.86	5.81
4th harmonic (%)	11.45	11.67	1.88
5th harmonic (%)	1.04	1.08	3.7
6th harmonic (%)	5.33	5.48	2.73

It must be noted that in Table 1 for the Fundamental's Amplitude relative error the value obtained on the microcontroller has been multiplied with 128 because of the scaling factor (0.5) used in the implemented FFT algorithm. The numerical value of harmonics is represented as percentage from the fundamental.

Table 1 data illustrates the errors introduced by the algorithm implemented on the microcontroller compared with the reference FFT algorithm implemented in LabVIEW that uses 64-bit doubles for operands and results.

From the results obtained and using voltage and current RMS the application is able to determine the power factor, apparent power, real power and the reactive power. These values are presented below (Table 2).

Table 2. Experimental results (Power)

Parameter	MSP	LabVIEW	Relative Error
Voltage RMS	1222.3	1222.3	0
Current RMS	1104.8	1104.8	0
Complex Power	1350397	1350397	0
cos(φ)	0.0725	0.0747	2.94
Real Power	97903.7	100874.6	2.94
Reactive Power	1346831	1346618	0.01

In Table 2 are presented in internal representation format, the data representing RMS values for the voltage and current. The power factor was computed using the phase difference between voltage and current fundamentals from the FFT results.

6.2 Performances

In the current configuration the microprocessor can compute up to 50 FFT algorithms per second. By analysing the data resulted from the FFT of the input signal the following information can be obtained: fundamental amplitude, harmonics (from 1 to 62) amplitude, voltage and current phase, apparent power, real power and reactive power.

From the obtained information the power quality phenomena that can be detected are shown in Table 3

Table 3 Detected power quality phenomena

Categories	Event	Notes
Short Duration Variations	Instantaneous Sag	>1cycle
	Instantaneous Swell	>1cycle
	Momentary Interruption	>1cycle
	Momentary Sag	
	Momentary Swell	
	Temporary Interruption	
	Temporary Sag	
	Temporary Swell	
Long Duration Variations	Sustained Interruption	
	Under Voltage	
	Over Voltage	
	Power Factor	
Waveform Distortion	Harmonics	

6.3 Errors and error sources

As shown by Szolik, *et al*., (2003) there are several error sources in the digital signal processing that influences the precision of the Power Quality parameters measurement like: quantisation error of ADC and truncation errors of FFT algorithm. In addition we identified some other sources of error that can affect the precision of the current application; these are presented below.

Finite word length and the 16-bit architecture is one of the most important error sources from this application. In order to maximize the execution speed we decided to use, in all the possible situations, 16-bit computations because these are native for the microcontroller's architecture and can be executed without the usage of library functions. To minimize the influence of this hardware limitation and to eliminate the possible overflows that could appear when calculating 16×16-bit multiplications we tried to used as much as possible the Hardware Multiplier.

Another source of errors is the quantization of the twiddle factors. In order to minimize the "on-line" computations required by the algorithm we pre-computed the twiddle factors and stored them in two arrays. To avoid floating-point operation we normalised these values by multiplication with 1024 and transformed them in 16-bit integers this operation can introduce additional imprecision. This solution can lead to further problems because of the possible overflow that could result. This is why we executed all multiplications with the twiddle factors on the Hardware Multiplier that has a 32-bit result register. The result obtained was re-scaled by right-shifting it with 10 bit-positions.

All errors that are related with the FFT algorithm implementation on the microcontroller are emphasized when the results are compared with reference values. In the Table 1 such comparison is made using results obtained in LabVIEW as reference.

The DC offset was needed in order to convert the negative portion of the waveform with the microcontroller's ADC that can digitize only positive voltages. This offset is later removed by software. A low quality offset signal can induce errors.

As in any other digital signal processing application the result is a compromise between speed precision and cost.

7. CONCLUSIONS

A very important feature for the application development is the ability to communicate with personal computer based software. This was particularly important when validating implemented solutions and evaluating errors introduced by the algorithm implementation. It also can be very useful in the future for further development because opens numerous opportunities for control, data-logging, data-analyzing and data-displaying.

This application is the result of a low-cost oriented approach for the Power Quality measurement problem and opens new perspectives because it demonstrates that a low-cost microcontroller with a flexible RISC architecture and an advanced algorithm implementation is capable to measure power quality parameters.

Because the increasingly importance of this domain for customers the producers are trying to provide more solutions to adapt their needs.

This application was intended to offer a different approach from the high-performance, expensive tools available on the market.

As presented above the results obtained are illustrative for the compromise solution between cost, speed and accuracy. The low-cost microcontroller provided limited resources and imposed some hardware restrictions. In order to obtain usable data after processing we tried to minimize as much as possible the negative effects of errors, implementation trade-offs, and to maximize the executions speed.

The FFT algorithm is an efficient computational scheme for the DFT and is commonly used in digital signal processing for the frequency analysis of a real analogue signal.

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