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Modernized Spaceborne GNSS Receivers

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Abstract: The further development of navigation receivers has to go hand in hand with the advances in the constellations for Global Navigation Satellite Systems (GNSS). As more and more features will be provided by the services of modernized GPS, GLONASS and the upcoming Galileo and COMPASS, the functions and performance of spaceborne GNSS receivers have to be extended as well. Today, the MosaicGNSS Receiver is operating in space using only the GPS L1 civil signal. Its successor, the LION Navigation Receiver, is currently under development for using all open civilian signals of GPS, Galileo and COMPASS.

1. INTRODUCTION

Parallel to the establishment of the Galileo system and the modernization of GPS space and ground segment, it is vital to build up the user segment as well. Galileo offers major advantages for the civil user community over present L1 C/A code GPS. For use on spacecraft, Galileo offers improved coverage, availability of over 99 %, high integrity of signals and, depending on the navigation processing, considerable improvement of navigation accuracy.

Main feature of Galileo, as well as in modernized GPS, is the transmission on several carrier frequencies spread out on a much wider frequency spectrum. The use of the multiple signals, e.g. E1, E5, and E6, allows elimination of ionospheres delays, which is one of the major error sources of present single frequency receivers and facilitates carrier based navigation for high precision and relative navigation applications.

A next generation GNSS receiver has to be capable of processing not only Galileo signals but also the GPS signals, leading to a total capability of up to six signals.

1.1 History and Present

About ten years ago, EADS Astrium started the development of GPS receivers for space applications. Key requirements for such a navigation receiver were low cost, low power consumption, low mass, small size, and radiation hardened components to withstand the space environment. Further more, there was a need for an easy access to all software for modifications and adaptations, even after launch. Since a hardware correlator for space application was not available on the European market at that time, a software based correlator for GPS signal reception using a digital signal processor (DSP) was developed. Resulting from this development was a software based sensor module, capable of receiving simultaneously the L1 C/A signal from up to eight GPS satellites (Botchkovski *et al.*, 1999).

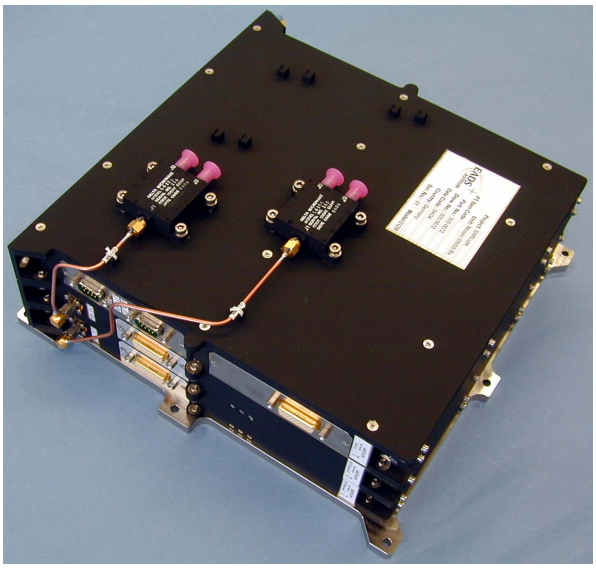

Fig. 1: Flight Unit Box of the MosaicGNSS Receiver

Today the then started MosaicGNSS Receiver is available as a product. It is shown in Fig. 1. It has been sold several times and several receivers are operating in space (Mittnacht *et al.*, 2004). Now the experience and knowledge gained, as much as the advances in the navigation signal technology push the development of a next generation of navigation receivers.

Stemming from a development performed in parallel by ESA is the AGGA-2 (Sinander *et al.*, 1998). This “Advanced GPS/ GLONASS ASIC” comprises 36 correlators implemented in hardware for servicing of twelve single frequency channels on both L1 and L2. Hence, a first extension of the MosaicGNSS receiver was swapping the correlation to the usage of the AGGA-2, e.g. for attitude determination by GPS. The data transfer between the correlator and the navigation algorithms was kept such that the navigation

module for solution and planning can be used for both, the hardware and the software correlator.

1.2 Future

The envisaged new navigation receiver has to cope both with multiple frequencies as well as with at least two independent navigation constellations, i.e. GPS and Galileo. To be available as the new heart for this class of navigation receivers, ESA initiated in 2002 a further development of the AGGA device, the AGGA-3, which stands now for the "Advanced GPS/Galileo ASIC". This chip comprises a GNSS core as well as a processor together with several communication interfaces in one ASIC. For providing the necessary processing power, the LEON-2 processor has been selected.

This hardware development requires a supplementing software development to have correctly working and tested algorithms available in time. Going well with the LEON family, the RTEMS operating system was selected to provide basic services. This platform was used to port all the existing functional modules to their new home.

During the port from the DSP to a LEON based system the separation of correlation and navigation was taken a step further to allow for a completely decoupled and fully modular system, with a dedicated extension to include external aiding data. In the following step, a breadboard consisting of a LEON-2 based FPGA board and an AGGA-2 based mezzanine is set up to allow for a stable laboratory environment.

2. MOSAIC GNSS RECEIVER

2.1 Receiver Hardware

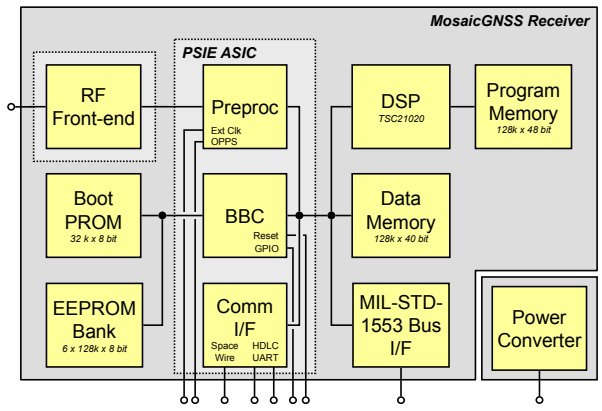

Fig. 2: Hardware Block Diagram of the MosaicGNSS Receiver

The block diagram given in Fig. 2 shows the hardware components of the MosaicGNSS Receiver. With no radiation hardened hardware correlators for space application available on the European market at the start of the development, the design is based on software correlation for GPS signal reception using a DSP board with the TSC21020 from Atmel. Based on the original ADSP-21020 from Analog Devices, this is a versatile high-performance DSP in radiation-tolerant technology, especially designed for aerospace systems and related hi-rel applications. The entire navigation receiver module comprises the DSP with SRAM for the program memory and data memory, a GPS PSIE ASIC, a boot PROM containing the primary boot loader, an EEPROM bank containing the GPS application software, and also one RF front-end. The GPS PSIE ASIC is a special development by EADS Astrium for GPS signal pre-conditioning and pre-processing, a board and boot control (BBC) and primary communication interfaces (UART, HDLC, SpaceWire). Working as a remote terminal, the MIL-STD-1553 bus interface is a further optional communication interface.

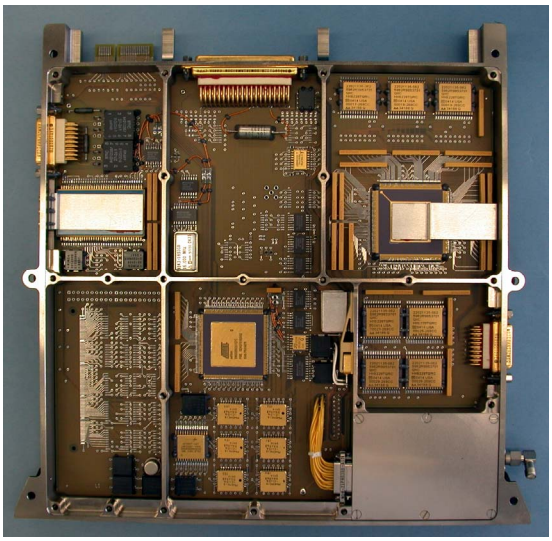

Fig. 3: Flight Module of the MosaicGNSS Receiver

A picture of the digital board of the navigation receiver flight module is given in Fig. 3. The DSP is sitting in the upper right section with SRAM chips above and below. Further SRAM chips are on the other side. The GPS PSIE ASIC is in the lower middle section together with the PROM and EEPROM chips; whereas the analog RF front-end occupies the lower right section. And as with all real hardware development, last minute patches are visible as well. The power converter has its own board (not shown in this article).

The complete navigation receiver box has been shown already in Fig. 1. For the commonly used redundancy in space, the box comprises two single MosaicGNSS Receiver modules together with their dedicated power supply and optional RF power combiners on top of the box for connecting two GPS antennas to each single navigation receiver module. These RF power combiners are only necessary, if the user satellite maintains an inertial attitude in LEO with no given satellite side looking up at the GPS constellation for all the time.

2.2 Receiver Software

A block diagram of the navigation receiver GPS application software is presented in Fig. 4. Highlighted are the two most important software modules, the *Sensor Module* and the *Navigation Module*.

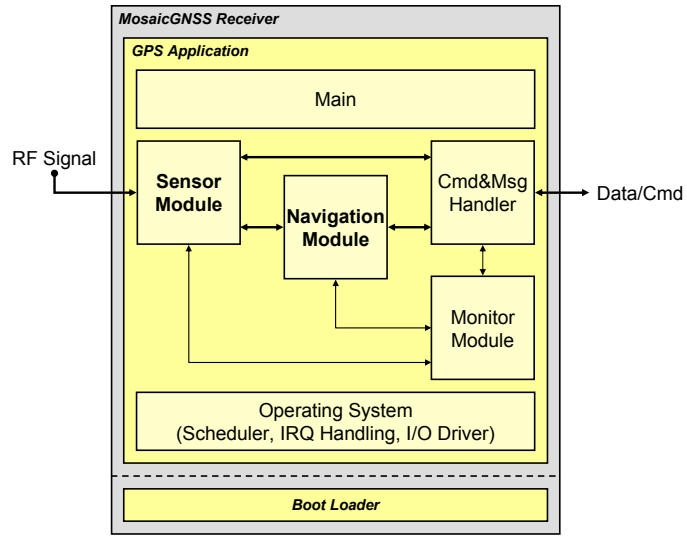

Fig. 4: Software Block Diagram of the MosaicGNSS Receiver

The *Sensor Module* contains all functions needed to receive GPS signals and to decode the GPS navigation message. The Sensor Module is commanded by the Navigation Module and it delivers raw measurement data of each tracked GPS satellite, comprising pseudorange, range rate, integrated Doppler, and signal to noise ratio. Furthermore, navigation data like GPS almanac and GPS ephemeris are provided.

The *Navigation Module* performs the navigation planning as well the navigation solution. The latter is available as kinematic point-solution or as Kalman-filtered dynamic solution. Any navigation solution consists of the information about position, velocity, and time (PVT).

Further software modules are the *Main Module* for initialization and executing of high level mode sequencing and switching, the *Monitor Module* for performing maintenance and debugging of all receiver functions, as well as generic FDIR functions and management of distributed FDIR functions. The *Command & Message Handler* provides the data communication interface between the internal modules on one side, and the user on the other side. The *Operating System* consists of a pre-emptive task scheduler, interrupt request handler, and the I/O drivers.

For loading the GPS application software from EEPROM as well as for providing patch & dump facilities, the *Boot Loader* is a separate piece of software.

2.3 Receiver Performance in Orbit

The first MosaicGNSS Receiver has been launched on board of a military radar reconnaissance system constellation in 2006. Among the further launches was also TerraSAR-X, a German radar satellite, which carries a high frequency X-band SAR sensor that can be operated in different modes, resolutions, and polarization.

At the very first start-up phase of the MosaicGNSS Receiver on the TerraSAR-X mission, the cold start time-to-first-fix (TTFF) was 459 seconds, which is well within the time range reached beforehand during simulation of various mission scenarios in the laboratory; see Tab. 1.

	TTFF [s]
Laboratory	345 – 489
In Orbit	459

Tab. 1: Time-to-first-fix of Cold Start

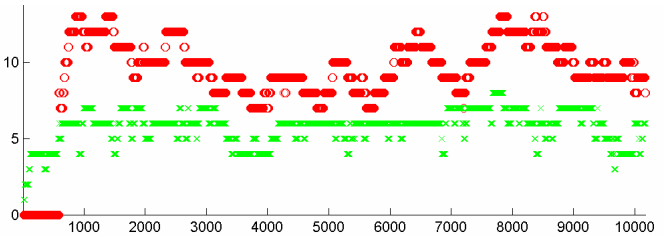

Fig. 5: Number of GPS Satellites over Run Time in Seconds: visible (red) compared with tracked (green)

The GPS almanac is collected during the TTFF and subsequently. With the almanac and once knowing its own position, the MosaicGNSS Receiver determines the visible GPS satellites. Fig. 5 compares their number, marked by the red circles, versus the number of GPS satellites acquired and in track, symbolized by the green x-markers. With up to eight GPS satellites simultaneous in track, the by design maximum number of eight channels is fully utilized.

RMS [m]	Day 1	Day 2	Day 1	Day 2
	Real-Time in Orbit		**Post-Processed on Ground**	
Radial	13.91	12.83	0.18	0.16
Along-track	6.63	6.29	0.41	0.39
Cross-track	5.90	6.27	0.32	0.61
3D	16.50	15.60	0.55	0.74

Tab. 2: Position Accuracy, RMS in [m]

Shortly after deployment of the TerraSAR-X satellite the position and velocity accuracy has been determined during two days without maneuvers (Montenbruck *et al.*, 2007). Additional precise orbit determination by post-processing the raw data on Ground, i.e. pseudorange and carrier phase measurements, leads to a RMS position accuracy of better than 1 m, see Tab. 2.

Std Dev [m]	Lab Test 1	Lab Test 2	Orbit Day 1	Orbit Day 2
Cross-track	2.50	2.41	5.77	6.17

Tab. 3: Cross-track Accuracy, Standard Deviation in [m]

As shown in Tab. 3, the standard deviation of the cross-track position error was found to be in orbit twice the value expected from laboratory simulation. By investigation of long term observations the cause was tracked down to a numerical

effect. Subsequently the flight software was optimized and tested and is now available as flight software.

RMS [m]	Test with Δ = 0 TEC	Orbit Day 1	Test with Δ = 10 TEC
Radial	4.90	13.91	17.89
Along-track	2.99	6.63	8.03
Cross-track	2.41	5.90	3.76
3D	6.23	16.50	19.97

Tab. 4: TEC-Dependency of Position Accuracy, RMS in [m]

The high radial error as seen in Tab. 2 results from ionospheric delays (Garcia-Fernàndez *et al.*, 2006). If the correct Total Electron Content (TEC) value is provided to the receiver, e.g. by telecommand, the effect can be drastically reduced. An example is given in Tab. 4, comparing the results from a test simulation with an ideally adapted TEC value (Δ = 0 TEC) to those present in the in-orbit evaluation and a dedicated test simulation with a mismatching delta of 10 TEC. As expected, the errors are largest in the radial direction.

2.4 Using a Hardware Correlator

In the past ESA initiated the development of a space borne hardware correlator yielding in the AGGA-2. The modular design of the MosaicGNSS Receiver allowed an easy substitution of its Sensor Module to use the AGGA-2 for comparison.

A corresponding AGGA-2 demonstrator breadboard was used for testing navigation performance as well as for testing attitude determination performance. The tests were performed using a GPS Simulator providing various orbit scenarios. The tests showed clearly, that specified performance requirements were fulfilled.

3. LION NAVIGATION RECEIVER

Advances in the navigation signal technology urge for the development of a next generation of navigation receivers. GPS is being modernized, providing more civil signals, and a first Galileo test satellite is already in orbit. Therefore, the envisaged new navigation receiver named "LION Navigation Receiver" has to cope both with multiple frequencies as well as with at least two independent navigation constellations.

The LION Navigation Receiver will be designed to make at least use of the GPS signals L1, L2C, and L5 and of the Galileo signals E1, E5a and E5b. As long as enough channels are available, the new navigation receiver will try to track all GPS and Galileo satellites in view. However, the number of channels, which can be implemented, depends on the size of the FPGA (laboratory model) and later-on on the size of the ASIC. A design goal for a first breadboard is to provide at least 18 single frequency channels, which can be coupled to 9 dual frequency channels.

The new navigation receiver will be designed to demodulate the navigation data messages of the GPS and Galileo navigation signals and to use this information for PVT determination through a instant point-solution as well as through a dynamic Kalman-filtered solution. The ambition is to reach sub-meter absolute position accuracy.

Concerning the timing of the pulse-per-second (PPS), using only GPS L1 C/A, the MosaicGNSS Receiver has already an 1 σ accuracy of 100 ns in LEO. The newer GNSS core will have a clock divider with a fractional part for the PPS output. With a PVT constellation of more than 4 visible satellites, a 1 σ result of less than 30 ns is considered to be feasible.

In addition to the typical cold start with the search-the-sky over all satellites of the GPS and Galileo constellations and typical warm start with a priori known PVT and almanac, a hot start based on additionally known ephemeris and an even faster reacquisition scheme will be implemented.

3.1 Receiver Hardware

Fig. 6 contains the hardware components of the new navigation receiver. It will be designed to be free of electronic parts controlled by International Traffic in Arms Regulations (ITAR) of the USA. Nevertheless, in the past it was not possible to get all the electronic parts with the required radiation tolerance from European sources. This problem might remain.

The power converter will provide power separately for the analog RF part including the clock oscillator and for the digital part, to prevent noise from the processing in the digital part spilling over into the analog part, especially into the clock oscillator.

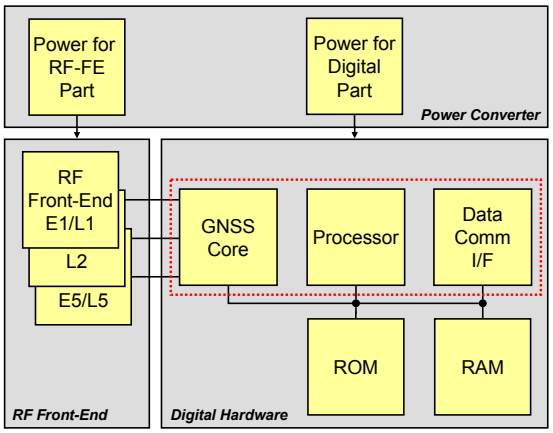

Fig. 6: Hardware Block Diagram of the Lion Navigation Receiver

In an RF front-end, the frequency down-conversion and the digitizing are two different functions. Some designs of an RF front-end have placed both into one single chip (e.g. GP2010 by Plessey), others into two separate chips (e.g. NJ1007R with NJ1017R by Nemerix). A single chip solution reduces the chip count, whereas a segmented solution provides a cleaner signal setup. Selection of the frequency band is typically done through a small number of external passive

components. Hence, up to three RF front-end modules will be necessary to obtain signals on E1/L1, L2, and E5/L5 of Galileo/GPS. In Europe, several companies like Chip Idea (Portugal), IMEC (Belgium), and Nemerix (Switzerland) have ongoing developments in this area. The architectural design of the new navigation receiver can be based on these new devices, being available already today or in near future.

#	GNSS Core	Processor	Comm I/F
1	Separate	Separate	Separate
2	Combined		Separate
3	Separate	Combined	
4	Combined		

Tab. 5: Combining Digital Hardware Features

Due to harsh space requirements, it is assumed for the next future, that neither memory for work (RAM) nor for storage (ROM) can be placed into an ASIC. So Tab. 5 summarizes possibilities to combine the different digital hardware building blocks into an ASIC. Another approach is the multi-chip module (MCM) technique, to be considered in a later development phase after consolidation of the used building blocks.

The first combination in line 1 leaves all components separate. Examples are the AGGA-2 for the GNSS core, the AT697E, an ASIC LEON-2 implementation available from Atmel, and some of the space qualified MIL-STD-1553 bus controller from DDC. Just having a GNSS core combined with a processor as shown in line 2 is not yet known to be published today, but line 3 combinations of processors with various communication interfaces are widely spread.

3.2 AGGA-3

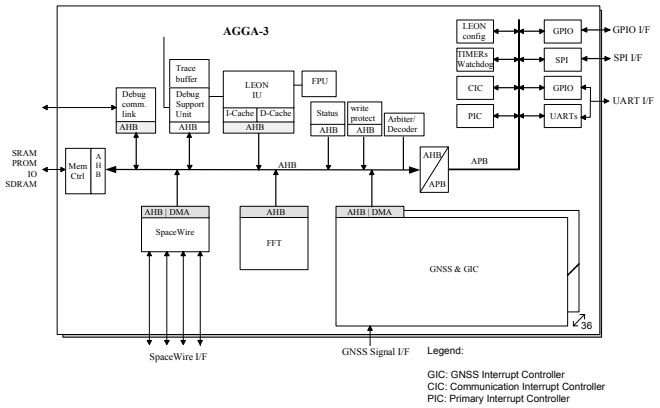

Fig. 7: Hardware Block Diagram of the AGGA-3

Very promising is the full combination of all three components, as it not only reduces the chip count to the most, but also allows for a faster data transfer between the different components within an ASIC instead going through external data lines on a PCB. The aforementioned AGGA-3 is such a development (Berberich *et al.*, 2004). Fig. 7 contains the block diagram of this ASIC. It includes a modern GNSS baseband processor, the LEON-FT as a fault-tolerant micro-processor with an IEEE-754 compliant FPU, an FFT module, UART interfaces, a SpaceWire module with four SpaceWire interfaces and a DSU SpaceWire interface.

The GNSS baseband processor (GNSS core) is capable of processing the current and future GPS signals L1 C/A, L2C, L5, L2 P(Y) and the open access Galileo signals that have shift register based codes and BOC(n,n) subcarrier.

The GNSS core includes digital down-conversion, beam-forming, enhanced power level detection, code and carrier loop aiding support, and optimized raw sampling for open-loop signal tracking. Codeless tracking of GPS L2 P(Y) signals is supported.

Each channel includes 5 complex code correlators, a dual integration stage for data, decryption or secondary code stripping, a secondary code sequencer, and a carrier and code aiding unit. The data from the GNSS baseband processor is transferred to memory by direct memory access (DMA). Two interrupt controllers assure the appropriate priority for data processing by the LEON processor. The time base generates the required clocks and assures the correct timing. The AGGA-3 includes a 128 point integer FFT module for e.g. fast signal acquisition support.

3.3 First Breadboard

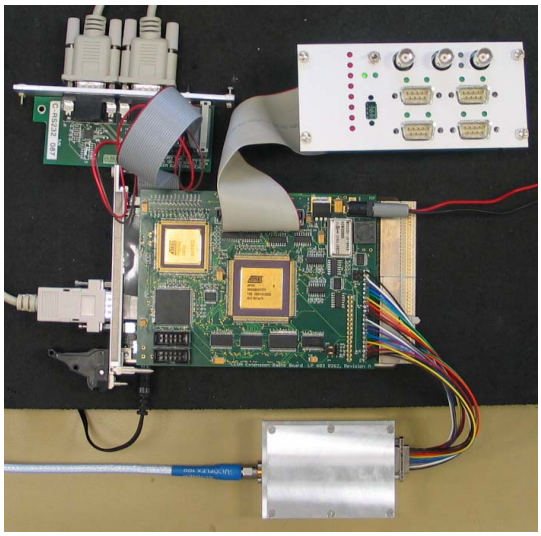

Fig. 8: Breadboard of the Lion Navigation Receiver

But before such a complex ASIC like the AGGA-3 is manufactured, the functionality of all components have to be tested thoroughly. The breadboard shown in Fig. 8 has still the three major components separated, i.e. its setup corresponds to line 1 of Tab. 5. The GNSS core is represented by the AGGA-2 and the communication interfaces are those of the GPS PSIE ASIC given in Fig. 2. The major change from the past development is the introduction of the LEON-2 as the processor for the new navigation receiver. The image of the LEON-2 is placed onto a FPGA board. This intermediate development step allows full evaluation of the LEON-2 capabilities for a new, next generation GNSS navigation single board receiver.

3.4 Receiver Software

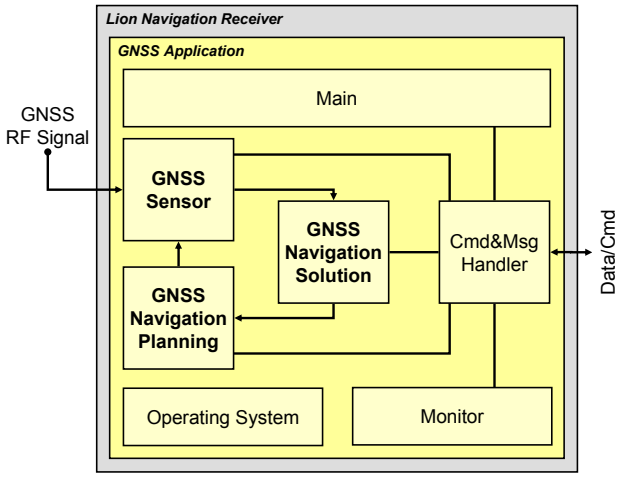

Fig. 9: Software Block Diagram of the Lion Navigation Receiver

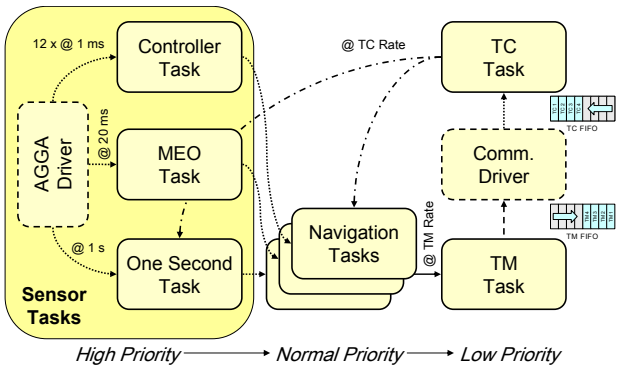

Fig. 10: Software Tasks of the Lion Navigation Receiver

The changes in the software from Fig. 4 to Fig. 9 are mainly in two fields. First it is the extension from GPS to GNSS and secondly it is the change of the Operating System.

The new *GNSS Sensor Module* has now to cope with all the new different signal formats and encoding, e.g. separation into data and pilot signal, or the usage of the new encoding named alternate modified binary offset (AltBOC). The new *GNSS Navigation Modules* for solution and planning have to combine all information from two different constellation systems. And to make the job a little bit more sophisticated, these constellation systems do no share the same time base. For the *Operating System* consisting of a pre-emptive task scheduler, interrupt request handler, and the I/O drivers, the RTEMS operating system was selected. The mapping of the functional modules into RTEMS tasks is shown in Fig. 10. The tasks associated with the GNSS Sensor Module are running with high priority. The Controller Task takes care of the twelve channels by performing GNSS signal acquisition and thereafter the signal tracking. At every measurement epoch (MEO), the MEO Task collects all raw measurements. Further signal processing is done every second by the One Second Task. The resulting data is handed over to the tasks of the GNSS Navigation Module. The preparation of telemetry output (TM) is in the responsibility of the TM task.On the other hand, incoming telecommand messages (TC) are checked by the TC task before the content is forwarded to a respective module. Hardware related processing is done in software drivers, written for the AGGA-2 chip as well as for any communication devices used in this system.

CONCLUSION

It is now the right time to develop the next generation of spaceborne navigation receivers, so that there are available for the customers in time with the deployment of the new GNSS constellations.

ACKNOWLEDGEMENTS

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The authors are responsible for the contents of this paper.

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