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Robust Filter Design for Sigma-Delta Modulators with One-Bit Quantizer and Analog Mismatch

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Abstract: A method for improving the signal-to-noise ratio (SNR) of single-stage sigma-delta modulators (SDMs) with one-bit quantizer is presented. It is well known that uncertainties and noises are sources of error which cause performance degradation. Specifically, the modulators are naturally subject to analog mismatch in capacitor values and finite amplifier gain, which are manifested as parametric uncertainties of the SDMs, whereas the quantization error due to the coarse quantizer is modeled as a bounded-peak additive noise. Robust stability margin optimization and suppression of the output swing of the non-ideal integrators are also considered in the integral design. Based on a frequently used linear model, we propose a new architecture for the SDMs. The associated digital filter is determined by robust control theory. For numerical illustration, comparisons between the proposed SDM and the conventional one are made. It is shown that the proposed SDM has an effective resolution of 16 bits.

1. INTRODUCTION

ΣΔ analog to digital converters (ADCs) have demonstrated to be an attractive solution for the implementation of analog-digital interfaces in systems consisting of analog and digital components. Compared to Nyquist-rate ADCs, ΣΔ architectures present a better performance in terms of resolution, speed and power consumption with more robustness against the imprecision in circuit and inherent noises (Cherry *et al*., 2000), (De La Rosa *et al*., 2002), (Medeiro *et al*., 1999). There are two architectures which are frequently used for SDMs: single-stage and multi-stage (or cascade or MASH) structures (Norsworthy *et al*., 1997). In order to achieve high resolution with low OSR and to enhance modulator stability, multi-bit quantizer is normally employed. However, like the inevitable mismatch of the analog components, the non-ideality of multi-bit quantization causes signal distortion and degrades the performance of the modulators. Recently, there are some research works presenting different digital techniques for correcting errors in mash ADC's, such as adaptive filter approach (Cauwenberghs *et al*., 2000), (Kiss *et al*., 2000), robust control approach (Gani, 2005), (Yang *et al*., 2006), and the other techniques (Leger *et al*., 2004), (Siragusa *et al*., 2000), (Plekhanov *et al*., 2003), (Yu, Shiang-Hwua, 2006). Stability analysis and design of a single-stage modulator using sliding mode control approach has been addressed in (Plekhanov *et al*., 2003), (Yu, Shiang-Hwua, 2006). In this work, we focus on a single-stage second-order SDM subject to analog imperfections, such as finite amplifier gain and capacitor value mismatch. Only one-bit quantizer is used. We propose to design a digital filter based on robust control theory to compensate the performance degradation due to the analog imperfection and the coarse quantizer, meanwhile, to improve the SNR.

The remainder of this paper is organised as follows. In Section 2, a brief review for ΣΔ modulators and robust control technique which will be used is provided. The design objectives of this paper are formally stated. In Section 3 we proposed a new architecture for the SDM with analog imperfections. These imperfections are modelled as parametric uncertainties. The control strategies are explained.

Finally, the digital filter design problem is cast in H-infinity control formulation and solved. The simulation results are presented in Section 4. Conclusions are provided in Section 5.

2. PRELIMINARIES AND PROBLEM STATEMENT

In this section, a brief introduction of the second-order sigma-delta modulators and the H_∞ control theory are presented. Next, the robust filter design problem we consider is formally stated.

2.1 Second-Order Sigma-Delta Modulators

A conventional second-order ΣΔ modulator is depicted in Fig. 1, where $H_j(z)$ $(j=1,2)$ are integrators; X denotes the input signal; E represents the quantization error; Y is the output signal; a_1, a_2, b_1, and b_2 are path coefficients. The signal transfer function (STF) and the noise transfer function (NTF) of the second-order ΣΔ modulator are defined as the transfer functions from the signals X and E to the output signal Y, respectively. Specifically,

$$\text{STF: } T_{YX}(z)=\frac{Y(z)}{X(z)}=\frac{a_1a_2H_1(z)H_2(z)}{1+a_1b_2H_1(z)H_2(z)+b_1H_2(z)} \qquad (1)$$

$$\text{NTF: } T_{YE}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + a_1 b_2 H_1(z) H_2(z) + b_1 H_2(z)} \quad (2)$$

Thus, the output Y reads

$$Y(z) = STF \times X(z) + NTF \times E(z). \quad (3)$$

Let $S_X(\omega)$ and $S_E(\omega)$ stand for the power spectral density (PSD) of input signal X and quantization error E, respectively, then the spectrum of the modulator output can be expressed by

$$S_Y(\omega) = \left|STF\right|^2 S_X(\omega) + \left|NTF\right|^2 S_E(\omega).$$

It follows that the powers of Y due to X and E are given respectively by

$$P_X = \int_{-f_b}^{f_b} \left|STF(f)\right|^2 S_X(f) df \cong \frac{\Delta^2 2^{2N}}{8} \quad (4)$$

$$P_E = \int_{-f_b}^{f_b} \left|NTF(f)\right|^2 S_E(f) df \cong \frac{\Delta^2 \pi^4}{60} \left(\frac{1}{OSR}\right)^5 \quad (5)$$

where f_b represents the baseband frequency, Δ is the quantization step, N is the order of the quantizer used, and OSR is the oversampling rate . Accordingly, the SNR of a second-order ΣΔ modulator is given by

$$SNR = 10\log\left(\frac{P_X}{P_E}\right) = 10\times\log\left(\frac{3}{2}2^{2N}\right) + 10\times\log\left(\frac{5}{\pi^4} OSR^5\right). \quad (6)$$

Equivalently,

$$SNR = 6.02N - 11.14 + 50\log OSR. \quad (7)$$

It is evident that the increase of the quantizer order N and/or the OSR would lead to higher SNR. But (7) is derived assuming perfect analog components. It is known that the ΣΔ modulator is, however, sensitive to imperfections in the analog components (Norsworthy *et al.*, 1997), (Cauwenberghs *et al.*, 2000). For example, two common sources of error are finite amplifier gain and mismatch in capacitor values, which are manifested as uncertainties in the gains and poles of the integrators (Norsworthy *et al.*, 1997), (Gani, 2005). The non-ideality of the integrators certainly would alter the transfer functions STF and NTF (see (1), (2)), consequently affecting the SNR performance (by (4)-(6)), which makes it difficult to establish a simple relationship between the factors. Worst of all, it degrades the performance.

2.2 A brief Review of the H_∞ Control Theory

H_∞ Control Theory (Zhou *et al.*, 1998) is a popular robust control technique which has been proved useful in many engineering applications. A popular controller synthesis paradigm is depicted in Fig. 2. The symbol P denotes the generalized plant including the nominal plant, weighting functions, etc, described by

$$P\begin{cases} x(k+1) = Ax(k) + B_1 w(k) + B_2 u(k) \\ z(k) = C_1 x(k) + D_{11} w(k) + D_{12} u(k) \\ y(k) = C_2 x(k) + D_{21} w(k) + D_{22} u(k) \end{cases}$$

where $x \in R^{n_P}$, $w \in R^{m_w}$, $u \in R^{m_u}$, $z \in R^{m_z}$, and $y \in R^{m_y}$.

The symbol K denotes a dynamic controller of the form

$$K\begin{cases} x_K(k+1) = A_K x_K(k) + B_K u(k) \\ y(k) = C_K x_K(k) + D_K u(k) \end{cases}$$

where $x_K \in R^{n_K}$, to be designed. w represents the exogenous inputs such as disturbances, reference commands, and the auxiliary signals from the uncertainties; z denotes the observed signal; the vector of measurements and control inputs are denoted by y and u , respectively. The so called optimal H_∞ control problem is to determine a stabilizing controller so that the closed-loop transfer function T_{zw} is minimized. A variety of engineering problems, such as robust stability margin optimization, noise attenuation, etc, can be cast into this formulation. Specifically, when there is a parametric perturbation Δ connecting z and w , and there exists a stabilizing controller K such that $\left\|T_{zw}\right\|_\infty < \gamma$, this implies that the robust stability margin is at least $1/\gamma$, i.e., the perturbed system remains stable when the size of the perturbation is no greater than $1/\gamma$. For the problem of noise attenuation with bounded peak noise w , for example the quantization error, minimization of the H_∞ norm of the transfer function T_{zw} leads to reduction of the power of z due to the noise.

2.3 Goal

The goal of this paper is, from the control's point of view, to design a robust digital filter to achieve the following objectives:

(a) **Robust Stability**: the closed-loop stability of the compensated ΣΔ modulator should be guaranteed for a range of parameter variations arising from analog mismatch, such as finite gain of the amplifiers and capacitor ratio mismatch.
(b) **Signal tracking**: the compensated ΣΔ modulator should be able to track the test sinusoidal input.
(c) **Noise attenuation**: the effect of the quantization error should be attenuated.

(d) **Output swing suppression**: The output of the critical integrator (the first one) is suppressed such that its peak value is below the integrator saturation level so as to prevent signal clipping.

Note that accomplishment of the objectives (b) and (c) is supposed to be able to improve the SNR, which will be explained in the sequel.

3. MAIN RESULTS

In this section we present a robust digital filter design for a second-order ΣΔ modulator with analog imperfections such as finite gain of the amplifiers and capacitor ratio mismatch. The proposed digital compensated system configuration is depicted in Fig. 3, where H_i, $i=1,2$, are the non-ideal (discrete-time) integrators due to the analog imperfections, and K is a robust digital filter to be determined. By experience, the first integrator H_i is the most critical part of the modulator. Therefore, the non-ideal integrator model is only assumed for the first integrator. Specifically,

$$H_1(z)=\frac{\beta z^{-1}}{1-\alpha z^{-1}}=\frac{(1-\delta_z)z^{-1}}{1-(1-\delta_p)z^{-1}} \tag{8}$$

$$H_2(z)=\frac{z^{-1}}{1-z^{-1}} \tag{9}$$

where $\delta_z \in [0,1)$ and $\delta_p \in [0,1)$ are deviations in the values of β and α (Gani, 2005). Note that $\delta_p = 1/A_V$ where A_V denotes the finite amplifier gain (Norsworthy *et al.*, 1997). Therefore, δ_p equals zero for the ideal case where A_V is infinite, and is usually a small positive number (less than one) for the cases where the amplifier gain is finite. We propose to design a digital filter that achieves the design objectives described in Section 2.3. For the purpose of signal tracking, an internal model K_{IM} expressed as

$$K_{IM}=\left(\frac{z^{-1}}{1-z^{-1}}\right)^2$$

which consists of two integrators is included in the robust filter K. With this, under the closed-loop stability assumption, the steady-state error $e(\infty)$ due to step or ramp type input X would be completely eliminated. Furthermore, making the error e small implies that the output Y keeps tracking the scaled input a_2X; hence the output is dominated by the input signal, which in turn implies good SNR. The quantization error arises from the operation of the quantizer is modelled as an additive bounded-peak disturbance added to the output of the second integrator. To reduce the output swing of the first integrator due to the quantization error, the idea is to minimize its contribution to the signal u_1 in the power sense; hence the power propagating through the first integrator is reduced. This can be done by designing a filter to minimize the H_∞ norm of the transfer function from E to u_1, i.e., T_{u_1E}. Similarly, the H_∞ norm of the transfer function T_{u_1X} is also to be minimized. For better loop characteristics, the weighing function W is introduced; see e.g., (Zhou *et al.*, 1998) for the details of the loop-shaping technique. On the other hand, minimizing the H_∞ norm of the transfer function $T_{z_\Delta w_\Delta}$ where $w_\Delta=[w_p \;\; w_z]^T$ and $z_\Delta=[z_p \;\; z_z]^T$ would increase the stability margin of the modulator.

In the following we invoke the H_∞ control theory to accomplish the control strategies discussed earlier. To this end, the proposed compensated ΣΔ modulator architecture is converted to the general synthesis framework in Fig. 2, where $x=[x_W \;\; x_1 \;\; x_2 \;\; x_{IM}]^T$ (represents a collection of the states of W, H_1, H_2, *and* K_{IM}), $z=[z_p \;\; z_z \;\; \tilde{u}_1 \;\; e]^T$, $w=[w_p \;\; w_z \;\; E \;\; X]^T$, $y=u_{K1}$, $u=Y$, $K=K_1$. The auxiliary signals w_z, w_p, z_z, z_p are related by the equation $w_\Delta=\Delta z_\Delta$, where

$$\Delta=\begin{bmatrix}\delta_p & 0\\ 0 & \delta_z\end{bmatrix}.$$

The generalized plant is given by

$$P \leftrightarrow \left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right] = \left[\begin{array}{c|c|c} A & B_1 & B_2 \\ \hline C_1 & D_{11} & D_{12} \\ \hline C_2 & D_{21} & D_{22} \end{array}\right]$$

with

$$A=\begin{bmatrix} A_W & 0 & -b_2B_WC_{H2} & 0 \\ 0 & A_{H1} & -b_2B_{H1}C_{H2} & 0 \\ 0 & a_1B_{H2}C_{H1} & A_{H2}-b_1B_{H2}C_{H2} & 0 \\ 0 & 0 & B_{IM}C_{H2} & A_{IM} \end{bmatrix}$$

$$B=\left[\begin{array}{cccc|c} 0 & 0 & -b_2B_W & a_2B_W & -B_W \\ 0 & -1 & -b_2B_{H1} & a_2B_{H1} & -1 \\ -a_1B_{H2} & 0 & -b_1B_{H2} & 0 & 0 \\ 0 & 0 & B_{IM} & 0 & 0 \end{array}\right]$$

$$C=\left[\begin{array}{cccc} 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ C_W & 0 & -b_2D_WC_{H2} & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & D_{IM}C_{H2} & C_{IM} \end{array}\right]$$

$$D=\left[\begin{array}{cccc|c} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -b_2D_W & a_2D_W & -D_W \\ 0 & 0 & 0 & a_2 & -1 \\ \hline 0 & 0 & D_{IM} & 0 & 0 \end{array}\right]$$

where we have used the following state-space representations

$$K_{IM} \leftrightarrow \begin{bmatrix} A_{IM} & B_{IM} \\ C_{IM} & D_{IM} \end{bmatrix},\; W \leftrightarrow \begin{bmatrix} A_W & B_W \\ C_W & D_W \end{bmatrix}$$

and $A_{H_i}=1$, $B_{H_i}=1$, $C_{H_i}=1, i=1,2$.

Accordingly, the robust digital filter design problem is formulated as the following H_∞ control problem:

$$\min_{K_1} \|T_{zw}\|_\infty \tag{10}$$

By the small gain theorem, if K_1 is determined such that the closed-loop system is stable and its H-infinity norm is less than γ, then it is guaranteed that the closed-loop system is stable against the uncertainties Δ with sizes not greater than $1/\gamma$. The problem can be efficiently solved by the MATLAB command dhinflmi (Gahinet *et al.*, 1995). The resulting filter is given by $K = K_1 K_{IM}$.

4. SIMULATIONS

In this section, numerical simulations are carried out and validated with MATLAB/SIMULINK for a second-order ΣΔ modulator with 1-bit quantizer (Gahinet *et al.*, 1995), (Schreier, 2004). Specifically, the modulator of this experiment is aimed at applying to an audio system with bandwidth 25 kHz. The over-sampling ratio (OSR) is chosen to be 256, and the path coefficients are chosen as $a_1=0.5$, $a_2=0.5$, $b_1=0.5$, and $b_2=0.5$. The output of the first integrator is limited to +1/-1. The test input signal is a 6250Hz sinusoidal wave whose amplitude is varied from -120 dB to 0 dB. The number of time points used for FFT is 65536. In addition, the weighting function W is chosen to be $(1+16z^{-1}+100z^{-2})/(1+1.21z^{-1}+0.79z^{-2})$. Solving the H_∞ control problem (10) yields the digital filter $K = K_1 K_{IM}$ where

$$K_1(z) = \frac{-0.1499z^{-1}+0.7129z^{-2}-1.303z^{-3}+1.226z^{-4}..}{1-0.6716z^{-1}+0.01049z^{-2}-0.1398z^{-3}-0.1112z^{-4}..} \\ \frac{-0.6427z^{-5}+0.1563z^{-6}}{+0.01188z^{-5}-0.1041z^{-6}}$$

The H_∞ norm of T_{zw} reads 290.5576 which in turn guarantees a conservative lower bound of the robust stability margin as 0.0034; that is, the compensated modulator remains stable at least for the range of deviations $\delta_z \in [0, 0.0034)$ and $\delta_p \in [0, 0.0034)$ in the values of β and α of the first integrator (see (8)), corresponding to insufficient op amplifier gain and capacitor ratio mismatch. In the following, three kinds of imperfections associated with integrator gains and poles are considered: (i) α=1-1/1000, β=1-1/1000; (ii) α=1-1/500, β=1-1/500; (iii) α=1-1/300, β=1-1/300. Note that in case (iii) α is close to the estimated stability margin. Table 1 shows the output swing range of the integrators and the SNR value for 0.1 volt input. It can be seen that for all of the three cases the worst case full-scale output swing range of the critical integrator (the first integrator) is reduced from 1.23 to 1.09 (11.38% reduction) by the proposed robust control technique. In Fig. 4, the results of the output power spectrum density (PSD) when the 6250Hz sinusoidal input with amplitude 0.1 volt is applied confirm good signal tracking and noise attenuation properties of the proposed robust SDM, which in turn gives better calibration than the conventional SDM. In particular, this is true for the case with more severe analog imperfections, i.e., case (iii). Furthermore, Fig. 5 show the resulting SNR versus input amplitude. It can be seen that in terms of SNR the proposed robust SDM outperforms the conventional SDM for various input amplitudes under consideration. In Table 2, it is shown that the peak SNR value of each individual case increases at least 10dB by the proposed robust control approach. By (7) this yields an effective resolution of 16 bits. We, therefore, conclude that the proposed robust SDM (with one-bit quantizer) provides a high performance design with less cost than the conventional SDM with multi-bit quantizer.

Table 1. Output swing, SNR values obtained using Matlab

(a) Conventional ΣΔ modulator

Uncertainty assumption	α=1-1/1000, β=1-1/1000	α=1-1/500, β=1-1/500	α=1-1/300, β=1-1/300
Output swing of 1st integrator	0.60 ~ -0.63	0.60 ~ -0.62	0.59 ~ -0.58
Output swing of 2nd integrator	0.77 ~ -0.78	0.76 ~ -0.78	0.76 ~ -0.75
SNR (dB)	76.1	75.3	75.5

(b) Robust ΣΔ modulator

Uncertainty assumption	α=1-1/1000, β=1-1/1000	α=1-1/500, β=1-1/500	α=1-1/300, β=1-1/300
Output swing of 1st integrator	0.54 ~ -0.55	0.54 ~ -0.54	0.54 ~ -0.54
Output swing of 2nd integrator	0.67 ~ -0.73	0.74 ~ -0.74	0.62 ~ -0.74
SNR (dB)	86.4	87.5	88.1

Table 2. Peak SNR value obtained using Matlab

Uncertainty assumption	α=1-1/1000, β=1-1/1000	α=1-1/500, β=1-1/500	α=1-1/300, β=1-1/300
Conventional ΣΔ modulator	86.657 @-5.78	86.315 @ -5.30	85.745 @ -5.30
Robust ΣΔ modulator	97.887 @ -0.60	98.446 @ -0.98	97.473 @ -0.91
Improvement in dB	12.96 %	14.05 %	13.68 %

5. CONCLUSIONS

A novel digital filter design has been presented for one-bit ΣΔ modulators subject to analog mismatch in capacitor values and finite amplifier gain. For simplicity, a second-order loop is considered. The problem of designing a digital filter to achieve high SNR and reduced signal swing for the SDM has been converted into a robust control problem of signal tracking and noise attenuation. New architecture based on internal model has been presented for signal tracking purpose, which together with the noise attenuation ability of the proposed scheme improves the SNR and suppresses the output swing of the critical integrator of the SDM. Simulation results for the cases of parameter excursions under consideration show that a 10-dB improvement in the SNR (over the conventional approach) can be obtained by the proposed approach. An effective resolution of 16 bits can be obtained for the cases of interest. Extension of the proposed approach to the higher order cases is straightforward.

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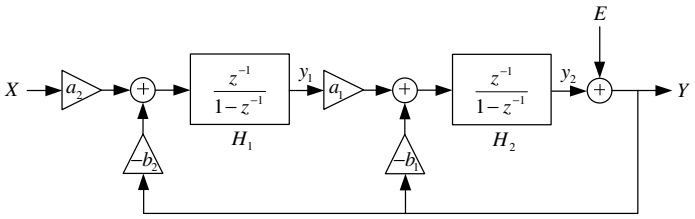


Fig. 1. Block diagram of a second-order ΣΔ modulator

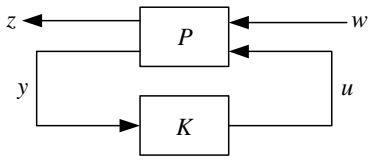


Fig. 2. General framework

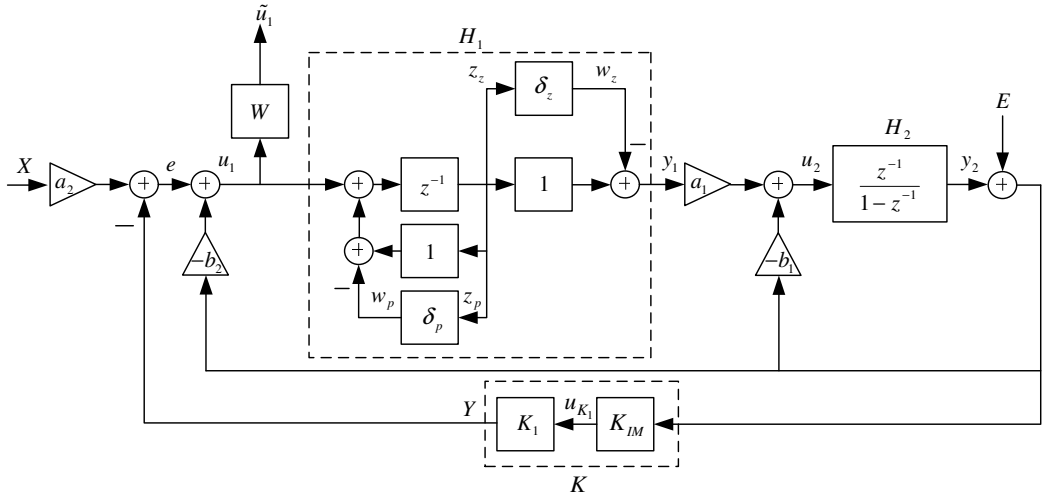
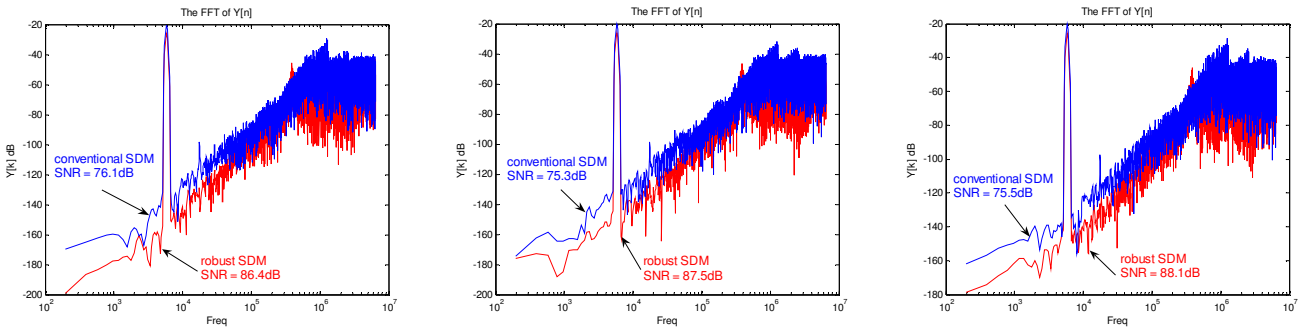
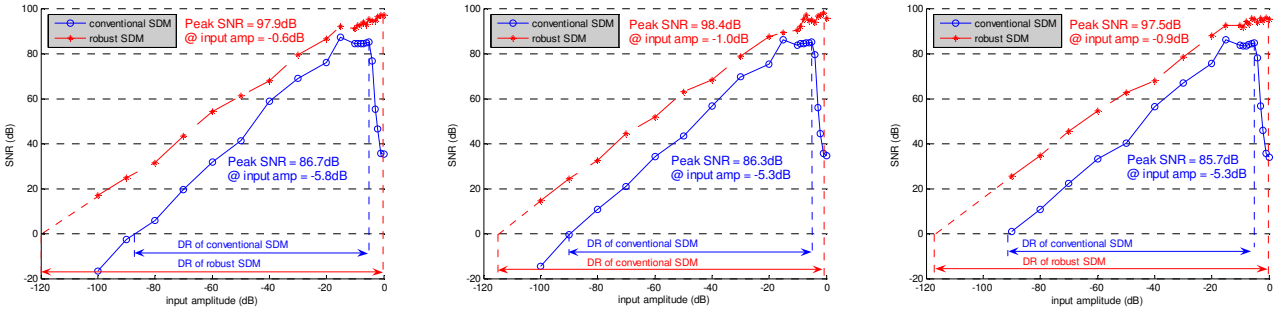


Fig. 3. The proposed scheme of second-order ΣΔ modulator



(a) case (i): α =1-1/1000, β =1-1/1000 (b) case (ii): α =1-1/500, β =1-1/500 (c) case (iii): α =1-1/300, β =1-1/300

Fig. 4. Power spectrum density associated with the conventional and the proposed robust ΣΔ modulators



(a) case (i): α =1-1/1000, β =1-1/1000 (b) case (ii): α =1-1/500, β =1-1/500 (c) case (iii): α =1-1/300, β =1-1/300

Fig. 5. Comparisons of SNR value and dynamic range associated with the conventional and the proposed robust ΣΔ modulators