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On the Implementation of a Wavelet-based Iterative Learning Controller Using CPLD/FPGA

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Abstract: The realization of a wavelet-based iterative learning controller (WILC) is presented in this paper. To meet the requirements of simplified hardware, fast rapid prototyping and fast up-date cycle, a wavelet-based iterative learning control system is implemented on a single FPGA (Field Programmable Gate Array) . There are three modules in this FPGA-based system, they are a feedback module, a discrete wavelet transform (DWT) module and an inverse discrete wavelet transform (IDWT) module. An external static random access memory (SRAM) is also employed to store the learning control signal processed by wavelet transform before updating the feedback control signal. To verify its effectiveness, a belt-driven ink-jet printer is adopted as the control target and a much improved speed-tracking performance is observed from the experimental verification. With the help of the learning process, the ink-jet printer needs no calibration during continuous operation and the velocity of the printer-head can be steadily running at 24 inch/sec.

1. INTRODUCTION

Iterative learning control (ILC) schemes have been widely used in systems that perform repeatable tasks, such as robot arm trajectory following and machine tools (Arimoto *et al.*, 1984, Atlson and McIntyre, 1986). The process of "learning" can overcome the "learnable" uncertainties that may not be taken care of by most conventional control techniques. However, for systems exhibit "unlearnable" dynamics such as dead zones, friction and external disturbances, the ILC schemes would eventually fail to work properly over the iterative process (Jang *et al.*, 1995, Elci *et al.*, 2002). In such applications with the help applying wavelet transform, the ILC is applicable to systems having unlearnable dynamics with a much enhanced performance (Tzeng *et al.*, 2005, 2006,). Wavelet transform (WT) has become a powerful tool for various signal-processing applications such as signal analysis, de-noising, communication and image processing (Grangetto *et al.*, 2002, Huang *et al.*, 2002). The advantage of WT is favoured over other transforms (esp. Fourier Transform) mainly from the fact that the WT performs a multi-resolution signal analysis in both time- and frequency-domain. Instead of transforming a pure 'time description' into a pure 'frequency description', WT offers the time-frequency description. Namely, with WT on the error signal, the learnable and unlearnable part can be separated. The stability of this wavelet-based iterative learning control (WILC) scheme has been reported in the authors' previous work (Tzeng and Chen 2005, Tzeng *et al.*, 2005, 2006,). The ILC algorithms have also been realized on various platforms (Tzeng and Chen 2005, Tzeng *et al.*, 2006), intensive computation in nature would always limit its application in systems that require continuous operation, however. In this article, we propose a single FPGA (10K-100RC240) by ALTERA Inc. to realize a WILC design for the speed control of a belt-driven ink-jet printer. As compared to the PC-based

realization, realization of the WILC scheme via FPGA has not been reported in the literature. Using the FPGA to realize WILC algorithm provides many advantages in real-time applications, such as simplified hardware, rapid prototyping and fast update cycle. In the implementation, an 8-bit data bus is adopted to simplify the hardware and to minimize the firmware loading. To verify the design, a belt-driven ink-jet printer is employed as the control target and a much improved speed-tracking performance is observed from the experimental verification. With the help of the learning process, the ink-jet printer needs no calibration during continuous operation and the velocity of the printer-head can be speed up to 24 inch/sec steadily.

2. THE SYSTEM ARCHITECTURE

The architecture of a WILC system is shown in Fig. 1, where y_d is the desired output trajectory and y_k is the system output at the *k*-th iteration.
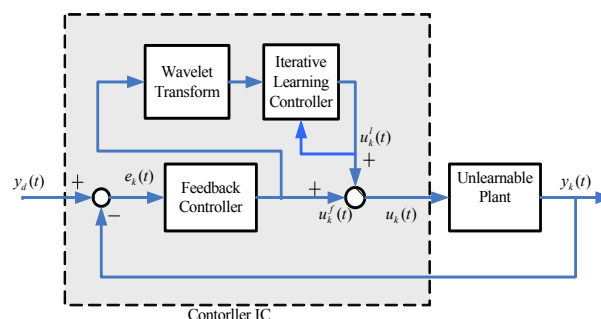

Fig. 1. Structure of the Wavelet-based Iterative Learning
Control (WILC) System

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The WILC scheme is expressed as follows.

$$u_k(t) = u_k^l(t) + u_k^f(t) \tag{1}$$

$$u_k^l(t) = u_{k-1}^l(t) + \alpha W * u_{k-1}^f \tag{2}$$

$$u_k^f(t) = \beta e_k(t) \tag{3}$$

Where α is a positive and fixed learning gain, (3) is a proportional feedback control law while u_k^l is the iterative learning control law. The feedback control signal u_k^f is processed by wavelet transform and then applied to update the learning profile for the next cycle of operation. The stability of the system has been proved in the previous work (Tzeng and Chen 2005). To yield satisfactory learning behaviour, both parameters of the controller, α and β, can be chosen according to the article (Tzeng and Chen 2005), which depends soly on the prior knowledge of the system and the performance index. Fig. 2 shows the block diagram of the over all system.
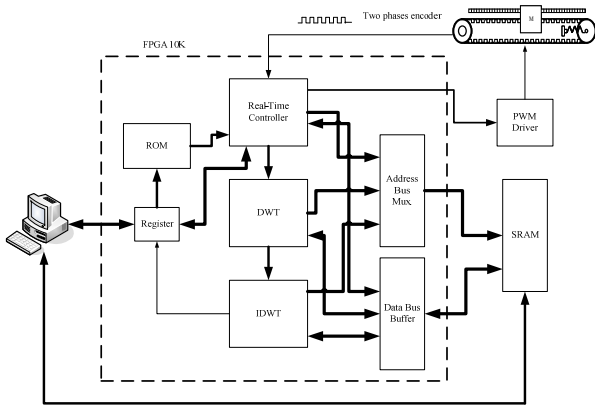
The detail functions of the three modules of the FPGA-based WILC system are described in certain detail as follows.

A. The Feedback Module

Fig. 3 shows the structure of the feedback module. This module consists of the over-sampling sub-module (Su, 1998), multiplier, bus & state control module and PWM generator module. A two-phase (a, b phase) position signal is detected by using the photo encoder and is then sent into the over-sampling sub-module.
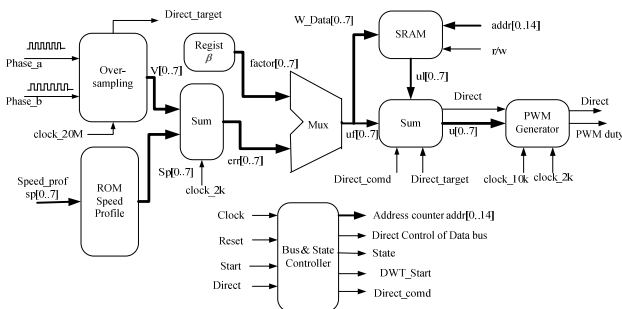

Fig. 3. Structure of the Feedback Module

The over-sampling sub-module utilizes a digital filter to filter out the positional noise and use a high frequency clock to count the number of pulse between two sampling pulses interval. The timing chart of the over-sampling is shown in Fig. 4.
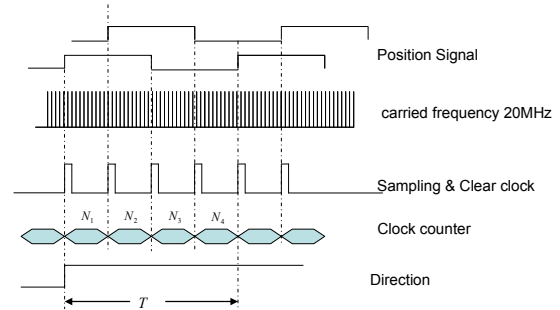

Fig.4 . The Timing Chart of the Over-sampling Sub-module

Where the down counter counts four times (N_1 to N_4) during the interval of T (T is the period of position signal) and the average speed is then calculated according to

$$\text{Target speed (inch/sec)} = \frac{N_1 + N_2 + N_3 + N_4}{4} \times D \tag{4}$$

B. The Discrete Wavelet Transform (DWT) Module

A typical two-level decomposition of the discrete wavelet transform is shown in Fig. 5. Through the same process, a N-level decomposition of DWT can be generated, where N is the number of frequency bands in which decomposed signals are situated.
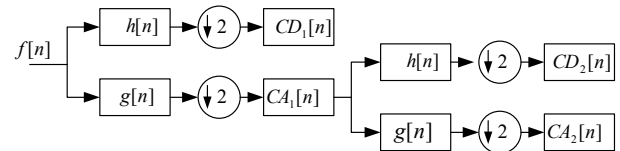

Fig. 5. A Two-level Discrete Wavelet Transform

The original signal f is fed into the low-pass filter $g[n]$ and the high-pass filter $h[n]$ which decompose the original signal into approximations coefficients, $CA_1[n]$ and details coefficients, $CD_1[n]$, respectively. The low-pass signal $CA_1[n]$ can be computed from the convolution of f with $g[n]$ plus a down-sampling with a factor of two. Similarly, through the high-pass filter $h[n]$ the details coefficients $CD_1[n]$ can be computed. Repeating this process, the approximations $CA_1[n]$ can be further decomposed into $CA_2[n]$ and $CD_2[n]$. This operation is formulated as follows.

$$\begin{aligned} CA_1 &= \text{down - two sampling } (f * g) \\ CD_1 &= \text{down - two sampling } (f * h) \end{aligned} \tag{5}$$

Where the down-two sampling is the mean of down sampling with a factor of two, and symbol * represents a convolution operator. In this paper, we utilize the learnable dynamics of

the control system to update the control signal that corresponds to the low frequency part of the feedback control signal in nature. Thus, we only need to compute the CA_m part, $m=1,2,...5$. Using the famous Daubechies 5/3 filter, the coefficients of low-pass filter are listed as below.

$$g = \frac{1}{8}[g[0] + g[1]z^{-1} + g[2]z^{-2} + g[3]z^{-3} + g[4]z^{-4}] \qquad (6)$$

Where $g[0] = -1, g[1] = 2, g[2] = 6, g[3] = 2, g[4] = -1$.

The Daubechies 5/3 filter has the advantage that all coefficients are integer so that it is easy to implement and yields lossless compression. The DWT module is shown in Fig. 6.
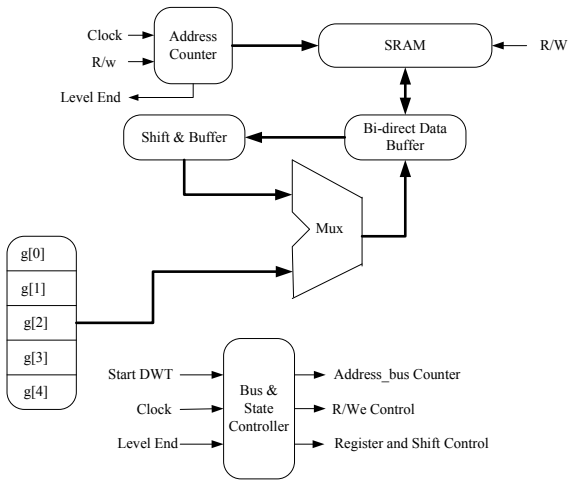

Fig. 6. Structure of the DWT Module

If a signal $f(i)$ is fed into the low-pass filter with a two-level stage, the output data from the first stage to the second stage can be expressed as follows.
The first stage

$$cA_1(0) = g(0)f(0) + g(1)f(-1) + g(2)f(-2) + g(3)f(-3) + g(4)f(-4)$$
$$cA_1(2) = g(0)f(2) + g(1)f(1) + g(2)f(0) + g(3)f(-1) + g(4)f(-2)$$
$$cA_1(4) = g(0)f(4) + g(1)f(3) + g(2)f(2) + g(3)f(1) + g(4)f(0)$$
$$cA_1(6) = g(0)f(6) + g(1)f(5) + g(2)f(4) + g(3)f(3) + g(4)f(2)$$
$$... \qquad ...$$
$$... \qquad ... \qquad (7)$$

The second stage

$$cA_2(0) = g(0)cA_1(0) + g(1)cA_1(-1) + g(2)cA_1(-2) + g(3)cA_1(-3) + g(4)cA_1(-4)$$
$$cA_2(2) = g(0)cA_1(2) + g(1)cA_1(1) + g(2)cA_1(0) + g(3)cA_1(-1) + g(4)cA_1(-2)$$
$$cA_2(4) = g(0)cA_1(4) + g(1)cA_1(3) + g(2)cA_1(2) + g(3)cA_1(1) + g(4)cA_1(0)$$
$$cA_2(6) = g(0)cA_1(6) + g(1)cA_2(5) + g(2)cA_1(4) + g(3)cA_1(3) + g(4)cA_1(2)$$
$$... \qquad ...$$
$$... \qquad ... \qquad (8)$$

Remark: Suppose that the cut-off frequency of the original signal f is ω_c. After applying a j-level DWT, the resultant approximation coefficient CA_i describes signal f in the frequency band from 0 to $2^{-j}\omega_c$, whereas the resultant detail coefficients CD_j describe signal f in the frequency band $2^{-j}\omega_c$ to $2^{-(j-1)}\omega_c$ (Fliege, 1994). Hence, the choice of the number of level of DWT is related to the frequency sub-band where the favorable information on the signal f is situated and the cut-off frequency of the original signal f. In our case, it is desired to filter out the learnable signal components, with the same frequency band as that of the command input, from the contaminated feedback signal. In engineering practice, the frequency response of the system is usually available. On the other hand, in this work, the frequency of the speed command profile is about 1 Hz and the resonant frequency of the ink-jet printer is measured to be 33 Hz. Thus, use of a five-level DWT is enough to filter out the useful signal components from the contaminated feedback signal.

C. The Inverse Discrete Wavelet Transform (IDWT) Module

Using the components of $CA_m[n]$ and $CD_m[n]$ to assemble back the original signal is the so called reconstruction process or synthesis process. The mathematical manipulation that accomplishes the synthesis is called the inverse discrete wavelet transform (IDWT). A two-level reconstruction of the inverse discrete wavelet transform is shown in Fig. 7. This process starts from an up-sampling with a factor of two which is so called up-two sampling.
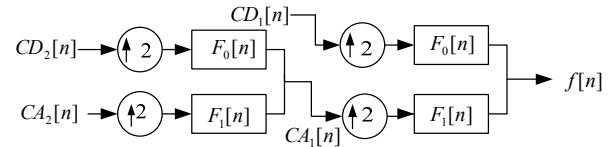

Fig. 7. Two-level Inverse Discrete Wavelet Transform

A typical method of the up-sampling is the process of lengthening a signal component by inserting zeros between samples. The detail coefficients $CD_2[n]$ are fed into the high-pass filter $F_0[n]$ and the approximations coefficients $CA_2[n]$ are fed into the low-pass filter $F_1[n]$ via the up-two sampling. The resultant outputs are then assembled back into the approximations coefficient $CA_1[n]$. The same process can be repeated until the original signal is completely reconstructed. In our design, only the low-pass filter $F_1[n]$ and the approximations coefficients $CA_m[n]$ are used to reconstruct the learnable part of the feedback control signal. The low-pass filter $F_1[n]$ is described as follows

$$F_1[n] = \frac{1}{2}[F_1[0] + F_1[1]z^{-1} + F_1[2]z^{-2}] \qquad (9)$$

Where $F_1[0]=1, F_1[1]=2, F_1[2]=1$.

The block diagram of the IDWT is as shown in Fig. 8. Since all the content of the SRAM is set to zeros while the system is started, the up-two sampling process can be realized by writing the coefficients to memory only with even addresses during IDWT.
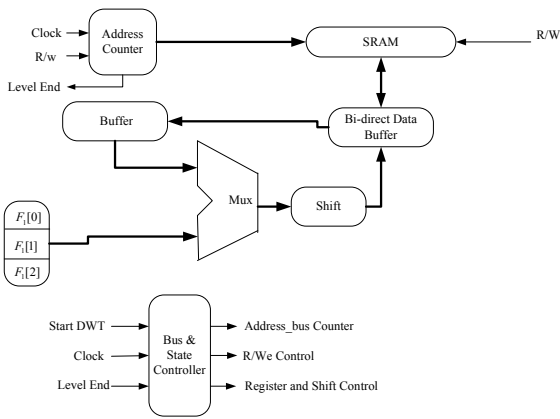
Fig. 8. Structure of the IDWT Module

3. REALIZATION OF THE WILC SYSTEM

While designing the FPGA-based system with the EDA tool, the synthesis, verification and implementation can be done with the same hardware description languages. Here, we chose the Max +plus II Ver.10.1 as the EDA tool and VHDL as the hardware description language. In this design, a host computer is communicated with the WILC IC through a dual 8255 interface card and a belt-driven ink-jet printer is employed as the target. Since the FPGA can only provide limited memory, an additional static random access memory (SRAM) is devised to store the control signal. The SRAM has an 8 bit data bus and a 15-bit address bus (8x32k bytes). These buses are controlled by the host computer so that the SRAM can be written or read through host computer itself or FPGA. Table 1 shows the mapping of the memory, in which uf_{k-1}^l and ub_{k-1}^l are the forward motion learning control signal and the backward motion learning control signal in previous cycle, respectively. In many repeatedly motion control e.g. ink-jet printer, the system dynamics are imbalanced for the forward motion and backward motion, namely, the forward and backward learning control signals are stored. In general, the learning control effort u_k^l is set to zero at the first iteration. Since the WILC system consists of the feedback law and the wavelet-based learning algorithm. The host computer sends out a command to the FPGA via the interface card, which can initiate and reset the FPGA, assign direction of the target motion, and control the bus. After the system is initiated by the host computer, the FPGA continually sends the system states back into the host computer and indicates that the WILC controller IC is busy or ready for the next task. In the WILC IC, the top block is the real-time feedback control module which carries out the speed and direction measurement by using an over-sampling module and feeds the synthesized control signal into a PWM driver. A pre-specified command profile is stored in the internal ROM of the FPGA using 1 K bytes of length and the system sampling rate is chosen to be 2K Hz. Once the real-time control process is activated, the feedback control signal

of previous cycle is reloaded to FPGA from the SARM and a five-level wavelet decomposition process is then executed. The bottom block performs the inverse discrete wavelet transform (IDWT). The inverse process includes the zeros padding, up-two sampling and convolution operation. In the reconstructing process, only the approximation coefficients (learnable part) is fed into the synthesis filter. The detail coefficients (unlearnable part) are excluded from feeding into the filter. The reconstructed signal is restored to SRAM as the updating the control signal for the next iteration cycle.

Table 1 The Address Mapping of the SRAM

Address	Signal Name	Description
0000~03FF	e_k	Error of the kth iteration
0400~07FF	u_k^f	Feedback Control Signal of the kth iteration
0800~0BFF	CA_1	Approximations Coefficients of Level 1.
0C00~0FFF	CA_2	Approximations Coefficients of Level 2.
1000~13FF	CA_3	Approximations Coefficients of Level 3.
1400~17FF	CA_4	Approximations Coefficients of Level 4.
1800~1BFF	CA_5	Approximations Coefficients of Level 5.
1C00~1FFF	uf_{k-1}^l	Learning Control Signal for Forward Motion
2000~23FF	ub_{k-1}^l	Learning Control Signal for Backward Motion

In this design, the three sub-modules operate at different frequencies. The highest frequency is set to be 20 MHz. The digital filter and down-counter built in the over-sampling module are worked at this frequency, while the operating frequency for the DWT and IDWT is set at 4 MHz and the PWM and sampling frequency are 10 kHz and 2 kHz, respectively. All of these frequencies are based on a 20MHz crystal oscillator. The components of the WILC (enclosed within the dashed box in Fig. 2) are all build inside a single Altera FLEX 10KRC-240 FPGA.

4. EXPERIMENTAL STUDY

According to (2) and (3), the control parameters α and β must be chosen. From our previous work(Tzeng and Chen 2005), when $\alpha=1$, the WILC scheme exhibits an sub-optimal learning behaviour. Using the Ziegler-Nichols method (Stefani *et al.*, 1994), we can show that when $\beta_{\max}=1.1$, the resonant phenomenon of the ink-jet printer would occur. Thus, for successful realization and satisfying the condition, $0 < \beta < \beta_{\max}$, we could select $\beta=1$. Furthermore,

by using system identification scheme in time-domain, an experimental transfer function (ETF) of the ink-jet printer can be obtained as

$$G(s) = \frac{188}{s + 28.8} \quad (\text{inch-per-second/volt}) \qquad (10)$$

A discretized pre-specified speed profile v_{ref} is also expressed as below.

$$v_{ref} = v_{max} \frac{1}{1 + e^{-\lambda(i-\gamma)}} \quad \text{inch/sec., } i = 0, 1, 2 \ldots N \qquad (11)$$

where i is the sampling number, v_{ref} is the reference speed of the printer-head (in inch/sec), λ is the reciprocal of time constant (in ms^{-1}) whose value will be constraint by the bandwidth (BW)of system, i.e. $\lambda < BW$. Once λ is determined, γ can be chosen based on the required distance for acceleration and deceleration. From (10), the corner frequency of the closed-loop system is around 216.8 rad/sec (about 34.5 Hz). Thus we can set $\lambda = 200 \, ms^{-1}$. Considering the power constraint of the dc motor, the terminal speed is selected as $v_{ref} = 24$ inch/sec. Consequently, the value of γ can be chosen based on the distance for acceleration and the acceleration time, e.g. 1 inch and 0.1 second, respectively, then we must determine $\gamma = 0.075$. The digitized speed profile is stored in the host computer with a 1K bytes (N=1023) memory and it is down-loaded to FPGA before the system is started. The sampling rate of the system is set to 2K Hz and the travelled distance of the printer-head is set at 8 inches within 0.512 second for an A4-size paper printing specification. The feedback control signal u_k^f is decomposed into five levels as shown in Fig.9. The signal A_5 is the low frequency part, corresponding to the learnable dynamics of the ink-jet printer system and the signals $D_1 \sim D_5$ are the high frequency part due to the unlearnable dynamics.
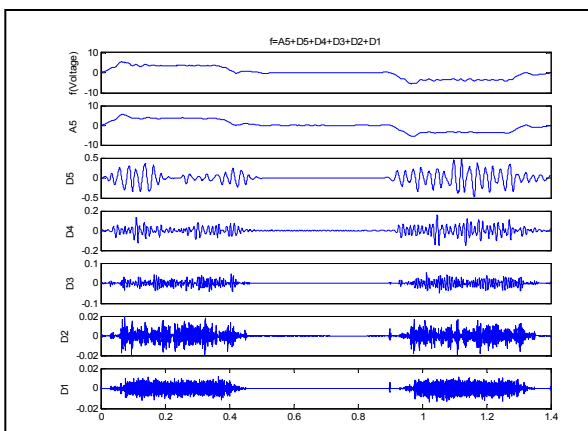

Fig. 9. The Wavelet Transformed Feedback Control Signal

At the 15th iteration, the speed tracking response and its tracking error of the ink-jet printer are shown in Fig. 10,

respectively. Table 2 shows the comparison of tracking error with various weight of the ink-tank. Obviously, the effect of the weight variation of the ink-tank from full (86g) to empty (41g) on tracking error is attenuated to a satisfactory range after a few iterations. This demonstrates that the WILC IC can automatically calibrate the tracking performance through iterative learning process.
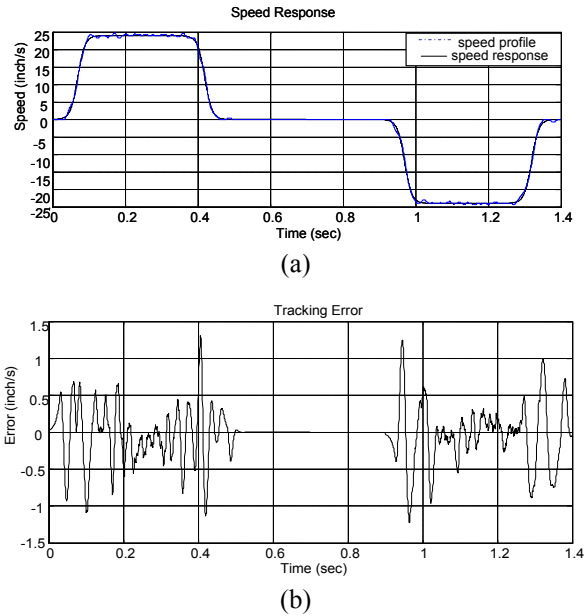

(a)

(b)

Fig. 10. (a) The Speed-tracking Profile. (b)Tracking Error at the 15th iteration.

Table 2 Tracking Error for Various Weight of the Ink-tank

Tank Status	Tank Weight (g)	No. of Iteration	Max Error (inch/s)	Error RMS (inch/s)
Full	86	15	1.68	0.19
Half	64	15	1.35	0.21
Empty	41	15	1.30	0.20

The comparisons of feedback control signal with five level of wavelet transform by using the FPGA-based WILC system and MATLAB Wavelet Tool box are shown in Fig 11(a) and (b), respectively and the results further demonstrate its efficacy in such application.

5. CONCLUSIONS

In this paper, we have developed an FPGA-based WILC system for a belt-driven motion control. The FPGA-based WILC system contains a feedback module and a wavelet-based iterative learning module. The FPGA-based WILC system can be incorporated with a personal computer to provide a total solution for high-performance motion control. A belt-driven ink-jet printer is employed as the control target. Using the proposed FPGA-based WILC system, given a pre-specified speed profile the ink-jet printer-head can achieve

high-speed tracking without inducing vibration under the influence of flexible timing-belt. In practical application, through the FPGA-based WILC system, the ink-jet printer speed control performance can be automatically tuned under the variation of the weight of the ink-tank.
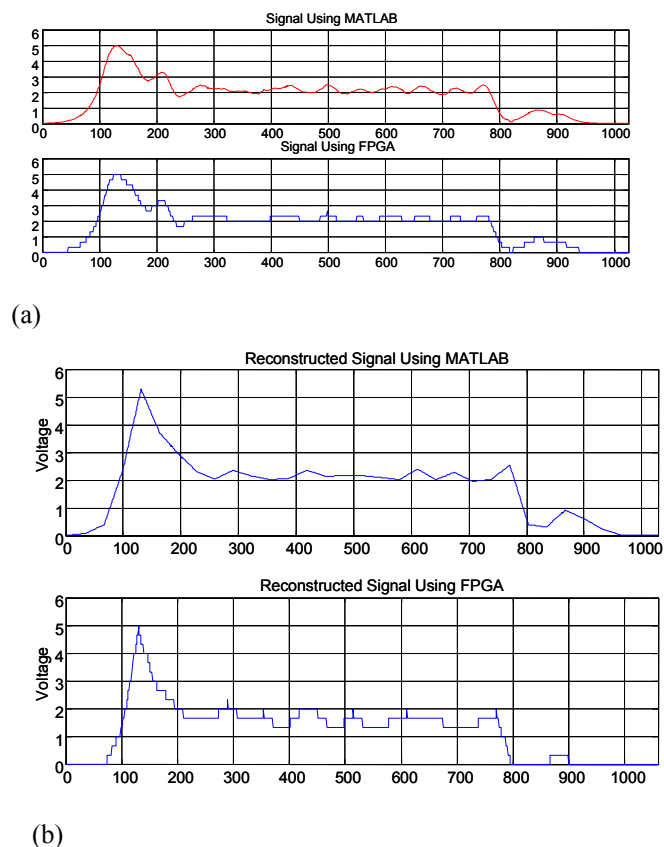

(a)

(b)

Fig. 11. MATLAB and FPGA Signal Comparison (a) The Original Signal. (b) The Reconstructed Signal

ACKNOWLEGEMENT

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