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Adaptive Nonlinear Control of Multiphase Synchronous Buck Power Converters

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Abstract: The problem of controlling multiphase synchronous buck power converters is considered. The aim is to regulate the output voltage of the converter and to ensure an adequate current sharing between its different channels. The control law is designed from the large-signal bilinear model (of the whole multi-channels converter) using the backstepping technique. The obtained regulator is shown to meet its objectives namely an asymptotic stability of the closed-loop system, a tight output voltage regulation, an adequate current sharing and a good estimation of load resistor.

1. INTRODUCTION

The rapid evolution in microprocessor technology poses new challenges for supplying power to these devices. The evolution began when the high-performance Pentium processor was created; this is driven by a non-standard, less-than-5-V power supply, instead of drawing its power from the 5V supply on the motherboard. In order to meet demands for faster and more efficient data processing, modern microprocessors are being designed with lower voltage implementations. The processor voltage supply in future generation processors will decrease below 1V. More devices will be packed on a single processor chip, and processors will operate at higher frequencies, beyond 3GHz. Therefore, microprocessors need aggressive power management. Future generation processors are expected to draw current up to 100 A. These demands, in turn, will necessitate special power supplies and Voltage Regulator Modules (VRMs) to provide lower voltages with higher currents and fast transient capabilities for microprocessors.

Meanwhile, as the speed of the processors increases, the dynamic loading of the VRMs significantly increase as well. Future microprocessors are expected to exhibit higher current slew rates of 5A/ns. These slew rates represent a severe problem for the large load changes that occur when the systems transfer from the sleep mode to the active mode, and vice versa. In this case, the parasitic impedance of the power supply connection to the load and the ESR and ESL of capacitors may cause a dramatic effect on VRM voltage (Zhang *et al*., 1996). If this impedance is not low enough, the supply voltage may fall out of the required range during the transient period. Moreover, the total voltage tolerance will be much tighter. Indeed, as the tolerance is 2% then, for a 1.1 V VRM output, the voltage deviation can only be ±33 mV. All these requirements pose serious design challenges.

Parallel connection of switching converters is an interesting technique both from practical and fundamental viewpoints (Chang *et al*., 1995, Perreault *et al*., 1997). The fact that that the converters share the output current is suitable for lower voltages with higher current capabilities in the next generation of microprocessors (Zhou *et al*., 2000, Panov *et al*., 2001). The sharing is also effective to improve reliability and fault tolerance. It also ensures the reduction of the output current ripple. This is convenient because it allows the reduction of the size and losses of the filtering stages. Finally, current sharing reduces the switching and conduction losses and electromagnetic interference (EMI).

Interleaved buck converters (IBC) are widely used in the personal computer industry in VRM applications to power central processing units, CPUs. This topology is widely used due to the reduced input and output capacitor ripple current that is gained by interleaving the converters as compared to a single buck power stage. The reduction in input and output capacitor RMS currents makes it possible to reduce the input and output capacitor banks needed for the design.

The parallel mode operation of dc-dc converters has been carried out using different control schemes (Luo *et al*., 1999, Balogh, 2002, Huang *et al*., 2003, Berbel *et al*., 2005, Saito *et al*., 2005, Abu-Qahouq *et al*., 2004). These seek a satisfactory output voltage regulation and load sharing.

The present paper focuses on the problem of controlling interleaved synchronous PWM buck converters. The controller is designed directly from the large-signal bilinear model of the whole system in which some of the converter parameters are submitted to uncertainty. More precisely, the load resistance varies extensively. An adaptive regulator design is then performed, using the backstepping technique, to achieve closed-loop stability, tight output voltage regulation, a fast transient response, an excellent current sharing among modules and a good estimation of load resistance. It is formally shown that the regulator thus

obtained actually meets the performances for which it has been designed.

The paper is organized as follows: in Section 2, the interleaved synchronous buck converter is described and modeled; Sections 3 and 4 are devoted to the controller theoretical and practical design; the controller stability and tracking performances are illustrated in Section 5. A conclusion and a reference list end the paper.

2. PRESENTATION AND MODELLING OF MULTIPHASE SYNCHRONOUS BUCK CONVERTER

Figure 1 shows the topology of a multiphase synchronous buck converter. It consists of N synchronous buck converters connected in parallel, sharing a common load represented by a pure resistor R which represents the microprocessor load. The k^{th} converter ($j = 1, ..., \mathrm{N}$) includes a synchronous switches, an inductance L_j and a capacitor C_j. Compared with conventional schottky diodes, synchronous switches are much more efficient, in applications necessitating high-current under low-voltage, because of their lower voltage drop. Each converter is controlled using interleaved PWM. A phase shift of $(360/N)$ degrees is introduced between each channel. The overall current of the converter will then be the addition of N pulsating currents, each with a $(360/N)$ phase. The ripple frequency of the total current will then be N times the fundamental switching frequency of a single converter. The total current ripple is therefore reduced compared to the current ripple of each converter. For a given current ripple, the interleaved channels allow much smaller and lighter inductances.

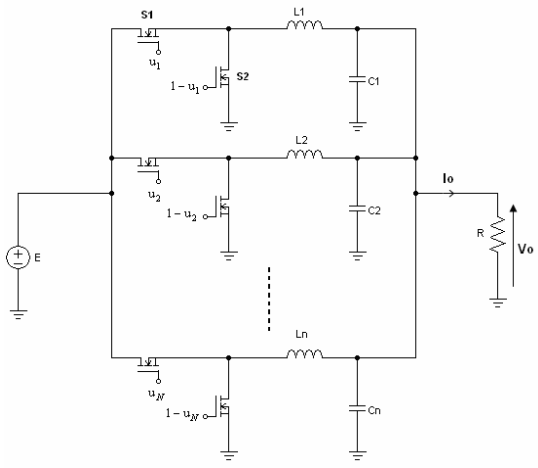

Fig. 1. Multi-phase interleaved buck converter

Figure 2 shows an averaged equivalent model of the k^{th} single synchronous buck converter, where R_1 and R_2 represent the RON of switches S1 and S2, respectively; r_{Lk} and r_{Ck} are the ESR values of L_k and C_k. Figure 2 also defines the control input u of the synchronous buck converter. This variable takes the discrete value $u = 1$ when switch S1 is on and S2 is off, and $u = 0$ when switch S1 is off and S2 is on. For simplicity, the ESL of C_k is not taken into account (as it only affects the high frequency spike, Berbel *et al.,* 2005). The current source ($i_T - i_{Lk}$) represents the sum of all supplied currents from the other cells. Considering identical inductances and capacitors, one has:

$$\begin{aligned} r_{L1} &= r_{L2} = ... = r_{LN} = r_L \\ r_{C1} &= r_{C2} = ... = r_{CN} = r_C \\ L_1 &= L_2 = ... = L_N = L \\ C_1 &= C_2 = ... = C_N = C \end{aligned} \tag{1}$$

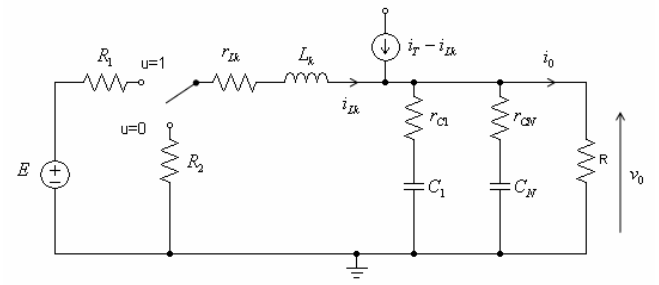

Fig.2. Equivalent circuit of a single buck converter.

Applying the Kirchoff's laws to the circuit of Fig.2, and using the averaging technique (Krein *et al.*, 1990) yield the following average model of the k^{th} converter:

$$\frac{d\bar{i}_{Lk}}{dt} = -\frac{1}{L}\left[R_L + R_2 + (R_1 - R_2)\mu_k\right]\bar{i}_{Lk} - \frac{1}{L}\bar{v}_0 + \frac{E}{L}\mu_k \tag{2a}$$

$$\frac{d\bar{v}_0}{dt} = \frac{1}{C_e}\bar{i}_T - \frac{1}{RC_e}\bar{v}_0 + \zeta(t) \tag{2b}$$

Where

$$\begin{aligned} \zeta(t) &= -\frac{R_C}{(R+R_C)C_e}\left(\bar{i}_T - \frac{\bar{v}_0}{R}\right) + (R_C \,//\, R)\frac{d\bar{i}_T}{dt} \\ &= R_C\left\{-\frac{1}{(R+R_C)}\left[\frac{R(R_L+R_2)}{L} + \frac{1}{C_e}\right]\bar{i}_T \right. \\ &\quad -\frac{1}{(R+R_C)}\left[\frac{NR}{L} - \frac{1}{RC_e}\right]\bar{v}_0 \\ &\quad \left. +\frac{R}{(R+R_C)L}\left[-(R_1-R_2)\sum_{k=1}^{N}\bar{i}_{Lk}\mu_k + E\sum_{k=1}^{N}\mu_k\right]\right\} \end{aligned} \tag{2c}$$

And

$$\bar{i}_T = \sum_{k=1}^{N}\bar{i}_{Lk} \tag{2d}$$

where N is the number of the units connected in parallel, $\bar{i}_{Lk}$ denotes the average value of the current in the inductance L_k, $\bar{v}_0$ is the average value of the output voltage, μ_k is the duty ratio which takes values in [0,1] and acts as the input control

variable of the k^{th} module. The parameters R_L, R_c and C_e are given as follows

$$R_L = r_L; \quad R_c = \frac{r_C}{N}; \quad C_e = \sum_{k=1}^{N} C_k = NC \tag{3}$$

The function $\zeta(t)$ acts as a perturbation term which is due to the presence of parasitic resistance of capacitors. Furthermore, the function $\zeta(t)$ converges, in steady state, to zero. For simplicity of the regulator design we take $\zeta(t) = 0$ in the next subsection.

3. ADAPTIVE CONTROL DESIGN AND STABILITY ANALYSIS

In the model (2), the load resistance R varies largely. This variations represent the changes that occur when the microprocessor transfer from the sleep mode to the active mode, and vice versa. To cope with such a model uncertainty the controller will be given a learning capacity. More specifically, the controller to be designed should involve an on-line estimation of the unknown parameter

$$\frac{1}{R} = \theta \tag{4}$$

The obtained estimate is denoted $\hat{\theta}$, it follows that

$$\theta = \hat{\theta} + \tilde{\theta} \tag{5}$$

where $\tilde{\theta}$ is the estimation error.

Recall that the control objectives are: (i) asymptotic stability of closed loop system, (ii) tight regulation of the voltage v_0, (iii) fast transient response, proper current sharing, (iv) good estimation of load resistance. To this end, an adaptive nonlinear regulator will be designed using the backstepping approach, (Krstić *et al*., 1995).

3.1 Adaptive regulator design

The second objective is to enforce the output voltage to track a given reference signal V_d despite the system parameter uncertainties. The reference signal and its two first derivatives are assumed to be known, bounded, and piecewise continuous. Following closely the backstepping technique, the controller is designed in two steps.

Step 1. Let us introduce the following tracking error:

$$z_1 = \bar{v}_0 - V_d \tag{6}$$

Achieving the tracking objective amounts to enforcing the error z_1 to vanish. To this end, the dynamics of z_1 have to be clearly defined. Deriving (6), it follows from (2b) that:

$$\dot{z}_1 = \frac{1}{C_e}\bar{i}_T - \frac{\theta}{C_e}\bar{v}_0 - \dot{V}_d \tag{7}$$

In the above equation, the quantity $\bar{i}_T / C_e$ stands as a virtual control variable. Let us consider the following Lyapunov function

$$V_1 = 0.5 z_1^2 + 0.5\tilde{\theta}^2 / \gamma \tag{8}$$

where $\gamma > 0$ is any real constant, called parameter adaptation gain. The time-derivative of V_1 along the trajectory of (7) is:

$$\dot{V}_1 = z_1\left(\frac{1}{C_e}\bar{i}_T + w_1\hat{\theta} - \dot{V}_d\right) - \frac{\tilde{\theta}}{\gamma}\left(\dot{\hat{\theta}} - \gamma w_1 z_1\right) \tag{9}$$

Where we have defined the first regressor function

$$w_1 = -\bar{v}_0 / C_e \tag{10}$$

We can eliminate $\tilde{\theta}$ from $\dot{V}_1$ with the update law $\dot{\hat{\theta}} = \gamma\tau_1$ where

$$\tau_1 = w_1 z_1 \tag{11}$$

Furthermore, z_1 can be regulated to zero if $\bar{i}_T / C_e = \alpha_1$ where α_1 is a stabilizing function defined by:

$$\alpha_1 = -w_1\hat{\theta} + \dot{V}_d - c_1 z_1 \tag{12}$$

where $c_1 > 0$ is a design parameter. Since $\bar{i}_T / C_e$ is not the actual control input, one can only seek the convergence of the error $\bar{i}_T / C_e - \alpha_1$ to zero, and we do not use $\dot{\hat{\theta}} = \gamma\tau_1$ as an update law. Instead we retain τ_1 as our first tuning function and tolerate the presence of $\tilde{\theta}$ in $\dot{V}_1$. Bearing in mind the current sharing requirement, we define the following second error variables:

$$z_{2k} = \bar{i}_{Lk} / C_e - \alpha_1 / N \qquad k = 1, \cdots, N \tag{13}$$

The next step is to determine a variation law for each control signal μ_k so that the set of errors z_1 and z_{2k} (k=1,…,N) vanish asymptotically. But, let us first establish some useful equations. Adding both sides of all equalities (13) yields, using (2d):

$$\sum_{j=1}^{N} z_{2k} = \bar{i}_T / C_e - \alpha_1 \tag{14}$$

Then, equation (7) becomes, using (12) and (14):

$$\dot{z}_1 = -c_1 z_1 + \sum_{k=1}^{N} z_{2k} + w_1\tilde{\theta} \tag{15}$$

Also, the derivative (9) of the Lyapunov function is rewritten:

$$\dot{V}_1 = -c_1 z_1^2 + z_1 \sum_{k=1}^{N} z_{2k} + \tilde{\theta}\left(\tau_1 - \dot{\hat{\theta}} / \gamma \right) \tag{16}$$

Step 2. The objective now is to enforce the error variables (z_1, z_{2k}) to vanish. To this end, let us first determine the dynamics of z_{2k}. Deriving (13) and using (2a), (12) and (15), one obtains:

$$\begin{aligned} \dot{z}_{2k} = & \frac{1}{LC_e}\left[E - (R_1 - R_2)\bar{i}_{Lk}\right]\mu_k + w_2\tilde{\theta} \\ & - \frac{1}{LC_e}(R_L + R_2)\bar{i}_{Lk} - \left(\frac{1}{LC_e} - \frac{\hat{\theta}^2}{NC_e^2} \right)\bar{v}_0 - \frac{\hat{\theta}}{NC_e^2}\bar{i}_T \\ & + \frac{w_1}{N}\dot{\hat{\theta}} - \frac{\ddot{V}_d}{N} - \frac{c_1^2}{N} z_1 + \frac{c_1}{N}\sum_{k=1}^{N} z_{2k} \end{aligned} \tag{17}$$

Where w_2 represents the second regressor function defined as follows

$$w_2 = (c_1 - \hat{\theta} / C_e) w_1 / N \tag{18}$$

In (17), the actual control inputs are in our disposal. We are finally in the position to design our update law and feedback controls to stabilize the full system, whose state vector is (z_1, z_{21}, ..., z_{2N}), with respect to

$$V = V_1 + \frac{1}{2}\sum_{j=1}^{N} z_{2j}^2 = \frac{1}{2} z_1^2 + \frac{1}{2\gamma}\tilde{\theta}^2 + \frac{1}{2}\sum_{k=1}^{N} z_{2k}^2 \tag{19}$$

Our goal is to make $\dot{V}$ nonpositive:

$$\begin{aligned} \dot{V} = & \dot{V}_1 + \sum_{k=1}^{N} z_{2k}\dot{z}_{2k} \\ & - c_1 z_1^2 + \sum_{k=1}^{N} z_{2k}\left\{ z_1 + \frac{1}{LC_e}\left[E - (R_1 - R_2)\bar{i}_{Lk}\right]\mu_k \right. \\ & - \frac{1}{LC_e}(R_L + R_2)\bar{i}_{Lk} - \left(\frac{1}{LC_e} - \frac{\hat{\theta}^2}{NC_e^2} \right)\bar{v}_0 \\ & \left. - \frac{\hat{\theta}}{NC_e^2}\bar{i}_T + \frac{w_1}{N}\dot{\hat{\theta}} - \frac{\ddot{V}_d}{N} - \frac{c_1^2}{N} z_1 + \frac{c_1}{N}\sum_{k=1}^{N} z_{2k} \right\} \\ & + \tilde{\theta}\left(\tau_1 + w_2 \sum_{k=1}^{N} z_{2k} - \frac{\dot{\hat{\theta}}}{\gamma} \right) \end{aligned} \tag{20}$$

To eliminate $\tilde{\theta}$ from $\dot{V}$ we choose the update law

$$\dot{\hat{\theta}} = \gamma\tau_2 \tag{21}$$

where:

$$\tau_2 = \tau_1 + w_2 \sum_{k=1}^{N} z_{2k} = Wz \tag{22}$$

is the second tuning function,

$$W = \left[w_1, w_2, w_2, \cdots, w_2 \right] \tag{23}$$

is the regressor vector, and

$$z = \left[z_1, z_{21}, z_{22}, \cdots, z_{2N} \right]^{\mathrm{T}} \tag{24}$$

is the error vector.

We choose the control μ_k to make the bracketed term in (20) multiplying z_{2k} equal to $-c_2 z_{2k}$

$$\begin{aligned} \mu_k = & \frac{LC_e}{(E - (R_1 - R_2)\bar{i}_{Lk})}\left\{ \frac{1}{LC_e}(R_L + R_2)\bar{i}_{Lk} \right. \\ & + \left(\frac{1}{LC_e} - \frac{\hat{\theta}^2}{NC_e^2} \right)\bar{v}_0 + \frac{\hat{\theta}}{NC_e^2}\bar{i}_T - \frac{w_1}{N}\gamma\tau_2 \\ & \left. + \frac{\ddot{V}_d}{N} + \left(\frac{c_1^2}{N} - 1 \right) z_1 - \frac{c_1}{N}\sum_{k=1}^{N} z_{2k} - c_2 z_{2k} \right\} \end{aligned} \tag{25}$$

where $c_2 > 0$ is a design parameter.

We rewrite (17), using (25), as follows

$$\dot{z}_{2k} = -c_2 z_{2k} - z_1 + w_2\tilde{\theta} \tag{26}$$

Finally, from (15), (26), (21) and (22) we obtain the following overall closed-loop system

$$\dot{z} = A_z z + W^T\tilde{\theta} \tag{27a}$$

$$\dot{\hat{\theta}} = \gamma W z \tag{27b}$$

where A_z is a skew symmetric matrix defined as follows

$$A_z = \begin{bmatrix} -c_1 & 1 & 1 & 1 & \cdots & 1 \\ -1 & -c_2 & 0 & 0 & \cdots & 0 \\ -1 & 0 & -c_2 & 0 & \cdots & 0 \\ -1 & 0 & 0 & -c_2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -1 & 0 & 0 & \cdots & 0 & -c_2 \end{bmatrix} \tag{27c}$$

3.2 Stability analysis

The stability of closed-loop system consisting of the controlled system (2) and the regulators (25) will now be

analyzed. Using (20) and (26), one gets the following derivative of the Lyapunov function V :

$$\dot{V} = -c_1 z_1^2 - c_2 \sum_{k=1}^{N} z_{2k}^2 \tag{28}$$

which shows that the equilibrium $(z, \tilde{\theta}) = 0$ is globally asymptotically stable.

From LaSalle's Invariance Theorem (Krstić *et al*., 1995), it further follows that the state $(z, \tilde{\theta})$ converges to the largest invariant set M of (27a)-(27b) contained in $E = \left\{(z, \tilde{\theta}) \in \mathrm{IR}^{N+2} / z = 0\right\}$, that is, in the set where $\dot{V} = 0$. This means, in particular, that $z(t) \to 0$ as $t \to \infty$.

Furthermore, on the invariant set M, we have $z \equiv 0$ and $\dot{z} \equiv 0$. Setting $z = 0$ and $\dot{z} = 0$ in (27a) and (27b) we obtain $\dot{\hat{\theta}} = 0$ and

$$W\tilde{\theta} = 0, \qquad \forall (z, \tilde{\theta}) \in M \tag{29}$$

On the other hand, in the light of (10), (18) and the fact that $\bar{v}_0 > 0$ for all $t > 0$ (the output voltage is practically positive) we can see that $W \neq 0$ for all $t > 0$. It follows, from (29), that

$$\tilde{\theta} = 0, \qquad \forall (z, \tilde{\theta}) \in M \tag{30}$$

which implies that $M = \{(0,0)\}$ and , in particular, we have

$\hat{\theta} \to \theta$ as $t \to \infty$.

The main result of this paper is then summarized in the following theorem

Theorem:

Consider the closed-loop system consisting of a multi-phase interleaved buck converter represented by (2a-b) subject to uncertain load resistor R , and the controller composed of the adaptive control law (25) and the parameter update law (21). Then, one has:

i) All the closed-loop signals remain bounded,
ii) The tracking error $z_1 = \bar{v}_0 - V_d$ converges to zero. This propriety ensures tight regulation under uncertainties.
iii) The estimation error $\tilde{\theta} = \theta - \hat{\theta}$ converges to zero.
iv) The errors $z_{2k} = \dfrac{\bar{i}_{Lk}}{C_e} - \dfrac{\alpha_1}{N}$ convergent to zero. This propriety ensures, in fact, the proper current sharing. □

4. SIMULATION RESULTS

The performances of the proposed adaptive control design are illustrated through simulations. The controlled system is a four phase synchronous buck converter with the characteristics of Table 1 (see user's guide of Evaluation Module TPS40090EVM-002 of Texas Instruments, available at: http://focus.ti.com/lit/ug/sluu195/sluu195.pdf).

Table 1: Parameters of the four phases synchronous buck converters

Parameter	Symbol	Value
Number of phases	N	4
Input voltage	E	12V
Inductance value	L	$0.62\mu H$
Inductance ESR	$R_L = r_L$	$1.75m\Omega$
Equivalent Capacitor value	C_e	$1800\mu F$
Capacitor ESR	R_c	$1.875m\Omega$
R-ON of switch S1	R_1	$4m\Omega$
R-ON of switch S2	R_2	$1.5m\Omega$
Switching frequency	f_s	$420kHz$

The experimental bench is described by Fig 3 and is simulated using the MATLAB software. The design parameters are chosen as follows: $c_1 = 11\text{x}10^4$, $c_2 = 8\text{x}10^4$ and $\gamma = 4\text{x}10^{-6}$. The behavior of such a system is illustrated by figures 4 to 6.

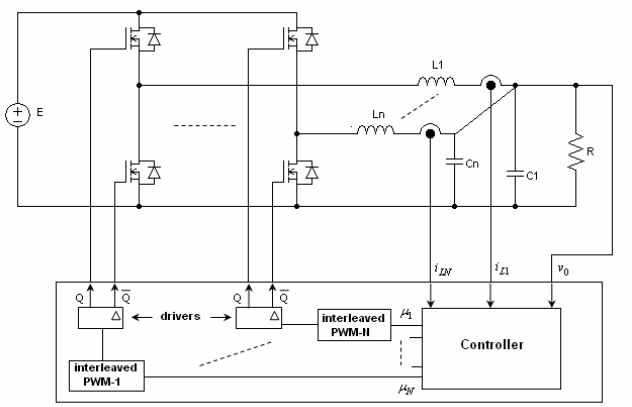

Fig. 3. Experimental bench for interleaved buck power converters

Fig. 4 illustrates the behavior of controlled system in presence of step reference $V_d = 1V$ and load changes. The changes are carried out between 0.01Ω and 0.05Ω, which corresponds to a variation of the output current from 20A to 100A. As it can be seen, despite the load resistor uncertainty, the controller behavior is satisfactory. It is worth noting that such a good behavior is preserved when facing different variations of the load resistance. This result confirms a tight regulation under uncertainties. Fig. 5 shows an appropriate current sharing between the interleaved inductor currents under load changes. Finally, Fig. 6 illustrates a perfect estimation of uncertain parameter.

6. CONCLUSIONS

The problem of controlling multiphase synchronous buck converters has been considered. The regulator is obtained from the nonlinear average model (2) using adaptive version of the backstepping approach. It is established, using a formal analysis and a simulation study, that the adaptive regulator thus obtained performs well in presence of changing load. Furthermore, the regulator provides a perfect tracking behavior and an excellent current sharing among modules.

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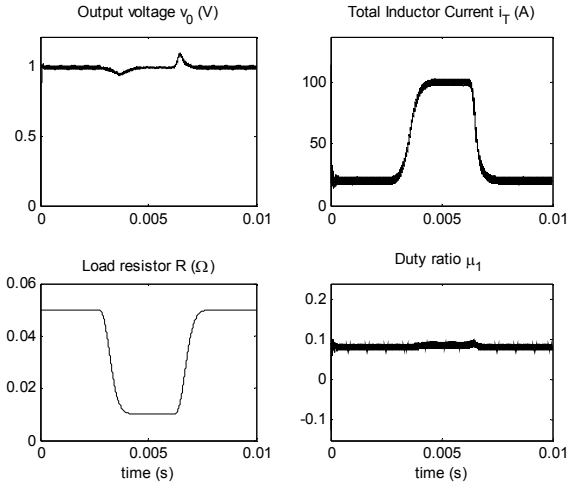

Fig 4: Controller behavior in presence of step reference V_d = 1V and load changes

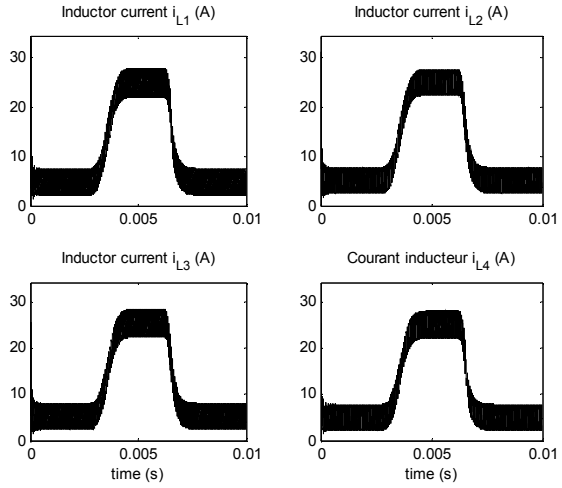

Fig. 5: Inductor currents in presence of load changes

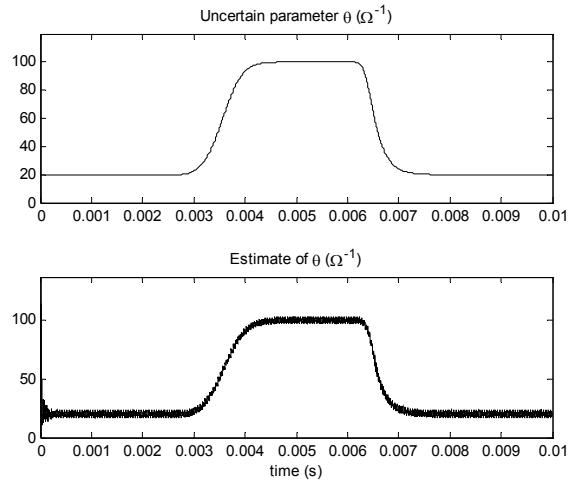

Fig 6: Uncertain parameter and its estimate