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Critical Dimension and Real-Time Temperature Control for Warped Wafers

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Abstract: In this paper, we present the experimental results on Critical Dimension (CD) control via real-time temperature control for warped wafers. As opposed to run-to-run control where information from the previous wafer or batch is used for control of the current wafer or batch, the approach here is real-time and make use of current information for control of the current wafer CD. In this paper we demonstrate that real-time control of the post-exposure bake temperature to give nonuniform temperature distribution across the warped wafer can reduce CD nonuniformity across the wafer.

1. INTRODUCTION

The key output in photolithography is the linewidth of the photoresist pattern or critical dimension (CD) and the CD is significantly impacted by several variables that must also be monitored to ensure quality [1]–[2].

Thermal processing of semiconductor substrate is common and critical in the photolithography sequence. Temperature uniformity control is an important issue with stringent specifications and has a significant impact on the CD [3]–[5]. The most temperature sensitive step in the photolithography sequence is the post-exposure bake step. As the photolithography industry moves to bigger substrate and smaller CD, the stringent requirements for post-exposure bake processing still persisted [6]. For commercially available deep ultraviolet resist, a representative post-exposure bake latitude for CD variation is 8 nm/°C [7]–[8]. A number of recent investigations also showed the importance of proper bake-plate operation on CD control [5], [9]–[10]

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake-plate for a given period of time. The heated bake-plate is usually held at a constant temperature by a feedback controller that adjusted the heater power in response to a temperature sensor embedded in the bake-plate near the surface. The wafers are usually placed on proximity pins of the order of 100 μm to create an air-gap to minimize contamination.

When a flat wafer at room temperature was placed on the bake-plate, the temperature of the bake-plate dropped at first but recovered gradually because of closed-loop control as shown in Figure 1(a). One challenge for thermal processing of wafers in photolithography is the warpage [11]. Figure 2(a) shows the bake-plate temperature when a wafer warped 140μm center-to-edge was dropped on the bake-plate. By comparing Figures 1(a) and 2(a), it can be seen that a flat and warped wafer gave rise to different magnitudes of bake-plate temperature drops due to different air-gap sizes and hence different thermal resistances between the substrates and bake-plate. Figure 3 shows a

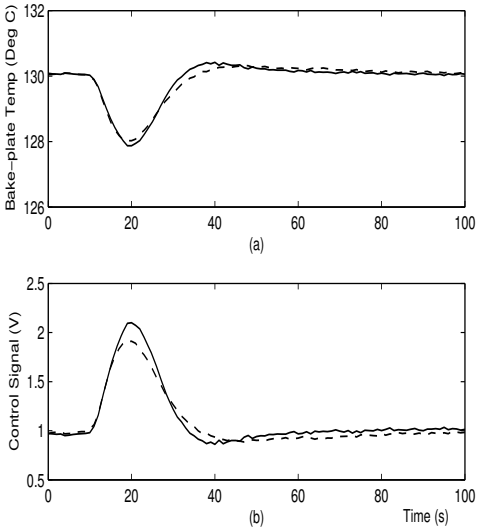

Fig. 1. Baking of Flat Wafer 1. Solid-line: center, Dashed-line: edge

flat and warped wafer on the bake-plate. Compared with the flat wafer, because the air-gaps between the warped wafer and bake-plate were bigger (smaller), the maximum temperature drops at the bake-plate were smaller (bigger). Furthermore, we expect the warped wafer to be heated to a lower (higher) temperature than the flat wafer. Finally, because of nonuniform processing condition, CD across the warped wafer was also not expected to be uniform.

It was demonstrated in [12]–[13] that the air-gap size can be estimated from the maximum bake-plate temperature drop through their inverse relationship. It was further demonstrated in [13] that using the heat transfer model of the baking system and the estimated air-gap, we can calculate for the bake-plate temperature to give uniform temperatures across the warped wafer. In this paper we extend the results by demonstrating that real-time control of the post-exposure bake temperature to give nonuniform temperature distribution across the warped wafer can re-

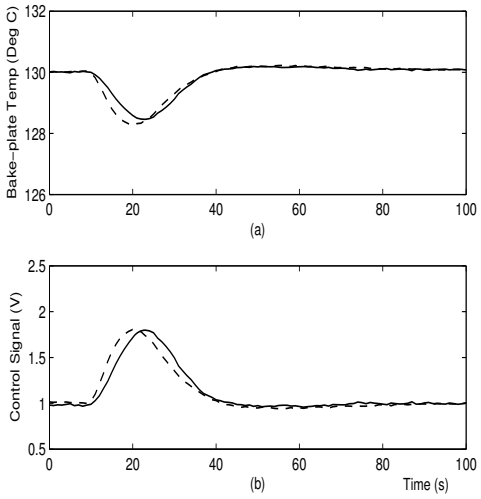

Fig. 2. Baking of Warped Wafer 4, Solid-line: center, Dashed-line: edge

duce CD nonuniformity. The proposed solution is to adjust the bake-plate temperature setpoints on-line and in real-time once warpage is detected. Warpage can differ from wafer to wafer and hence not expected to be repeatable. If warpage was repeatable then we could have fixed the bake-plate setpoints.

2. THERMAL MODELING OF THE BAKING PROCESS

The distributed thermal processing system used in this work consisted of two heating zones, center and edge as shown in Figure 3. Embedded within each of the heating zones were resistive heating elements and temperature sensors. The zones were separated by a small air-gap of approximately 1 mm for thermal insulation.

Spatial distributions of temperature and other quantities in a silicon wafer are most naturally expressed in a cylindrical coordinate system. We assume that the substrate used for baking is a silicon wafer and the bake-plate is cylindrical in shape with the same diameter as the wafer. Energy balances on the wafer and bake-plate can be carried out to obtain a two dimensional model as follows.

$$C_{w1}\dot{T}_{w1}(t) = \frac{T_{p1}(t)-T_{w1}(t)}{R_{a1}} + \frac{T_{w2}(t)-T_{w1}(t)}{R_{w12}} - \frac{T_{w1}(t)}{R_{w1}} \quad (1)$$

$$C_{w2}\dot{T}_{w2}(t) = \frac{T_{p2}(t)-T_{w2}(t)}{R_{a2}} + \frac{T_{w1}(t)-T_{w2}(t)}{R_{w12}} - \frac{T_{w2}(t)}{R_{w2}} \quad (2)$$

$$C_{p1}\dot{T}_{p1}(t) = u_1(t) + \frac{T_{p2}(t)-T_{p1}(t)}{R_{p12}} + \frac{T_{w1}(t)-T_{p1}(t)}{R_{a1}} - \frac{T_{p1}(t)}{R_{p1}} \quad (3)$$

$$C_{p2}\dot{T}_{p2}(t) = u_2(t) + \frac{T_{p1}(t)-T_{p2}(t)}{R_{p12}} + \frac{T_{w2}(t)-T_{p2}(t)}{R_{a2}} - \frac{T_{p2}(t)}{R_{p2}} \quad (4)$$

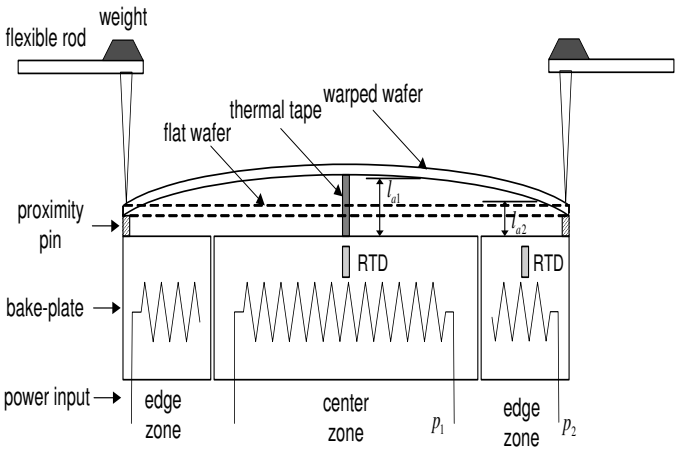

Fig. 3. Baking of Wafer

Table 1. Thermophysical Properties

	Property	Value
Wafer (silicon)	Density, ρ_w	2330 kg/m^3
	Specific heat capacity, c_w	850 J/kgK
	Diameter, d	100 mm
	Thickness, t_w	500 μm
Bake -plate	inner zone radius, r_1	30 mm
	outer zone radius, r_2	50 mm
Air	Thermal conductivity, k_a	0.03 W/mK
	Convective heat transfer coefficient, h	8 W/m^{2}K

Table 2. Thermal Capacitances and Resistances.

Thermal Capacitance & Resistance	Value	
R_{p1}	22.2 K/W	experimental
R_{p2}	6.3 K/W	experimental
R_{p12}	16.08 K/W	experimental
R_{w1}	44.21 K/W	$\frac{1}{h\pi r_1^2}$
R_{w2}	24.11 K/W	$\frac{1}{h\pi(r_2^2-r_1^2+dt_w)}$
R_{w12}	9.52 K/W	experimental
R_{a1}	changes with warpage	$\frac{l_{a1}}{k_a\pi r_1^2}$
R_{a2}	changes with warpage	$\frac{l_{a2}}{k_a\pi(r_2^2-r_1^2)}$
C_{p1}	101.2 J/K	experimental
C_{p2}	165.8 J/K	experimental
C_{w1}	2.8 J/K	$\rho_w c_w t_w \pi r_1^2$
C_{w2}	4.98 J/K	$\rho_w c_w t_w \pi\left(r_2^2-r_1^2\right)$

where subscripts p, w, a, 1 and 2 denote bake-plate, wafer, air-gap, center zone and edge zone respectively. Temperature above ambient, thermal capacitance and resistance are given by T, C and R respectively. Thermophysical properties of silicon and air can be obtained from handbooks [14] as tabulated in Table 1 and standard heat transfer experiments [12]–[13] can be conducted to determine most of the thermal capacitance and resistance values in Table 2.

A control software system was developed using the National Instruments LabView programming environment [15]. Two proportional-integral controllers of the following form were used to control the two zones of the bake-plate.

$$u_1(t) = K_{c1}\left(e_1(t) + \frac{1}{T_{I1}}\int e_1(t)dt\right) \quad (5)$$

$$u_2(t) = K_{c2}\left(e_2(t) + \frac{1}{T_{I2}}\int e_2(t)dt\right) \quad (6)$$

$$e_1(t) = T_{p1}(\infty) - T_{p1}(t)$$

$$e_2(t) = T_{p2}(\infty) - T_{p2}(t)$$

where $u_1(t)$, $u_2(t)$ are the control powers and $T_{p1}(\infty)$, $T_{p2}(\infty)$ are the bake-plate temperature setpoints. The proportional-integral controller parameters for the center and edge zones were manually tuned as $K_{c1} = 5.15$, $T_{I1} = 150$ and $K_{c2} = 16.79$, $T_{I2} = 500$ respectively.

The relationship between the steady-state wafer temperatures $T_{w1}(\infty)$, $T_{w2}(\infty)$ and bake-plate setpoints, $T_{p1}(\infty)$, $T_{p2}(\infty)$ for the two-zone system can be obtained from Equations (1) and (2) as

$$T_{p1}(\infty) = R_{a1}\left(\frac{1}{R_{T1}}T_{w1}(\infty) - \frac{1}{R_{w12}}T_{w2}(\infty)\right) \quad (7)$$

$$T_{p2}(\infty) = R_{a2}\left(\frac{1}{R_{T2}}T_{w2}(\infty) - \frac{1}{R_{w12}}T_{w1}(\infty)\right) \quad (8)$$

where

$$R_{T1} = \frac{R_{w1}R_{a1}R_{w12}}{R_{a1}R_{w12} + R_{w1}R_{w12} + R_{w1}R_{a1}}$$

$$R_{T2} = \frac{R_{w2}R_{a2}R_{w12}}{R_{a2}R_{w12} + R_{w2}R_{w12} + R_{w2}R_{a2}}$$

3. EXPERIMENT

3.1 Setup

In all our experiments, commercial chemical amplified resist, Shipley UV3 was spin-coated at 6000 revolutions per minute on a 4-inch wafer. After a post-apply bake, the wafer went through an exposure tool with a patterned mask of regularly spaced lines. The exposed photoresist was then baked, developed and the final output was the linewidth of the photoresist pattern or CD. Except for the real-time on-line adjustment of the post-exposure bake temperature, all other inputs to the photolithography processes such as spin speed, baking time, exposure dose, develop time etc. were kept constant. No anti-reflection coating was used. The post-exposure bake-time was fixed at 90s.

The experimental setup for the post-exposure bake of a warped wafer is shown in Figure 3. We ensured a fixed warpage during the baking experiment by mechanically pressing the edges of the wafer against the proximity pins of 70μm. The center-to-edge warpage was given by the difference between the height of proximity pin and thermal tape thickness.

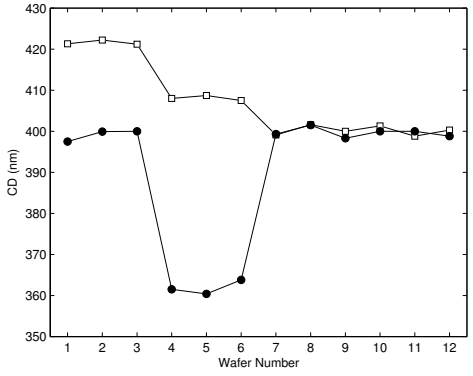

Fig. 4. Critical dimension measurements. Circle: center; Square: edge; Wafer 1–3: flat wafer with conventional baking; Wafer 4–6: warped wafer with conventional baking; Wafer 7–9: flat wafer with optimized baking; Wafer 10–12: warped wafer with real-time on-line adjustment of bake-plate temperature setpoints

3.2 Runs

Twelve Experiment (Wafer) Runs were performed. On each wafer we monitored CD at 2 points, 1.5 inches apart, one near the center, the other near the edge of the wafer. At each point, three samples of linewidths were measured by scanning electron microscope to give the average CD in Figure 4. The results for Runs 1, 4, 7, 10 are tabulated in Table 3 for further discussion. The other runs were repeat experiments. Wafers 1–3 and 7–9 were flat while 4–6 and 10–12 were warped 140μm center-to-edge.

Because photoresist was coated on the patterned wafer, it was not convenient to attach temperature sensors on the wafer to measure wafer temperature. To do so, another set of experiments with the same wafer warpage and bake-plate setpoints were conducted. There were no pattern nor photoresist on these wafers and their sole purpose was for us to obtain the wafer temperatures. Resistance Temperature Detectors (RTD) were attached to the wafers [16, 17] for temperature measurements. Thermal grease was applied to the RTD sensors for better heat transfer. The measured wafer temperatures are included in the last row of Table 3 and in the column that corresponded to the warpage and bake-plate setpoints. Figure 5 shows the measured wafer temperature for a warped wafer. The wafer was baked for 90s starting from $t = 10$s.

The bake-plate temperature curve for Flat Wafer 1 is shown in Figure 1. Notice in Table 3 that for Flat Wafer 1 even though the wafer temperature at center (128.1°C) and edge (128.0°C) were approximately equal. CD nonuniformity was 23nm. This can be expected as properties at center and edge may not be the same e.g. the thickness of the coat of photoresist across the wafer is known to be nonuniform [18]–[19]. Nonuniform photoresist thickness can cause nonuniform CD through a swing curve effect [20]–[22]. In [13] the bake-plate temperatures were controlled to give uniform temperatures on the wafer. We demonstrated here that this is not good enough to give uniform CD. Nonuniform temperature distribution across the wafer may be required to obtain uniform CD at center and edge.

Table 3. Experimental Results

Experiment (Wafer) No.		1	4	7	10
Warpage		Flat	Warp	Flat	Warp
Bake-plate Setpoint (°C)	Center	130	130	130.3	130.3 change to 133.6
$T_p(\infty) + T_a^*$	Edge	130	130	128.5	128.5 change to 129.6
Bake-plate Maximum	Center	2.13	1.54	2.12	1.54
Temperature Drop (°C)	Edge	1.98	1.73	1.98	1.70
CD (nm)	Center	399	362	399	399
	Edge	422	408	400	400
	Nonuniformity†	23	46	1	1
Wafer Temperature (°C)	Center	128.1	125.4	128.2	128.2
$T_w(\infty) + T_a^*$	Edge	128.0	126.9	126.6	126.6

*Ambient temperature $T_a = 24.5$°C.
†Difference between center and edge CD.

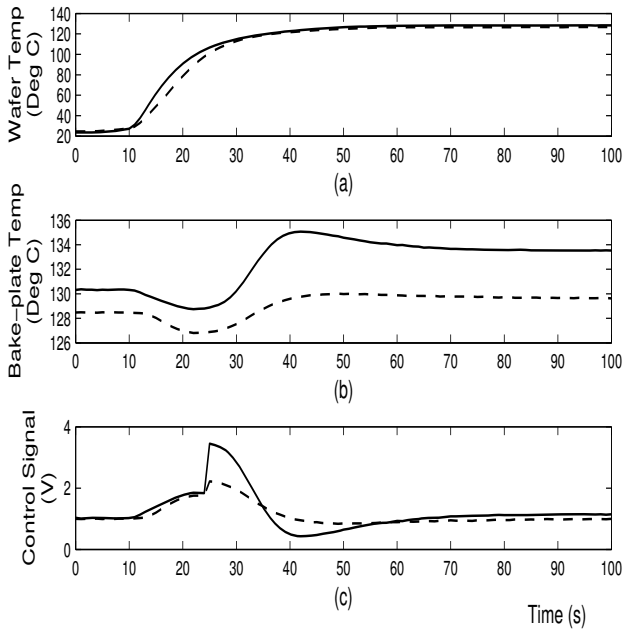

Fig. 5. Temperature measurement on a warped wafer with no photoresist nor pattern. Solid-line: center, Dashed-line: edge

The bake-plate temperature curve for Warped Wafer 4 is shown in Figure 2. Table 3 shows that the wafer center temperature (125.4°C) was lower than edge (126.9°C) and the CD nonuniformity doubled to 46 nm.

The manufacturing process should be fairly repeatable. In practice we expect a certain degree of repeatability of the CD profile and hence the two-zone bake-plate should start baking at different temperatures for different zones. Once a new set of bake-plate setpoints (130.3°C and 128.5°C) was implemented as shown in Figure 6, the CD non-uniformity on the Flat Wafer 7 was reduced to 1 nm as shown in Table 3. Notice that for CD uniformity, wafer temperature at center (128.2°C) was higher than edge (126.6°C).

3.3 Real-Time Control

For the given bake-plate, all parameters in Table 2 are known except for R_{a1} and R_{a2} which depended on wafer warpage or average air-gaps at center-zone (l_{a1}) and edge-zone (l_{a2}). The center and edge zones were pre-programmed to start baking at setpoints of 130.3°C and 128.5°C respectively to give desired wafer temperatures of

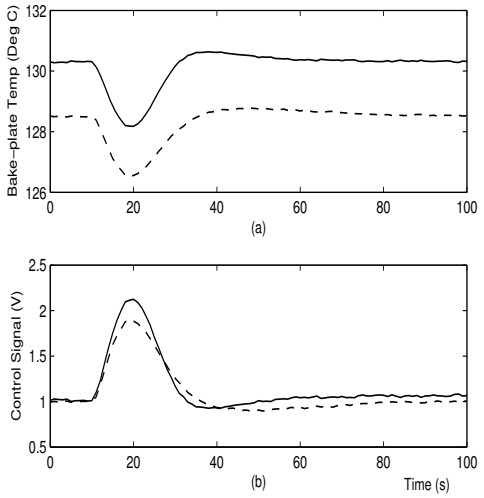

Fig. 6. Bake-plate setpoint adjusted to give uniform CD for Flat Wafer 7. Solid-line: center, Dashed-line: edge

$T_{w1}(\infty) + T_a = 128.2$°C and $T_{w2}(\infty) + T_a = 126.6$°C and CD uniformity for flat wafers. Equations (1) to (6) were solved to determine the maximum temperature drops in T_{p1} and T_{p2} for $20\mu\text{m} \le l_{a1} \le 300\mu\text{m}$ and $20\mu\text{m} \le l_{a2} \le 300\mu\text{m}$ and the results are plotted in Figures 7 and 8 for l_{a1} and l_{a2} respectively. They can also be tabulated to facilitate on-line search for l_{a1} and l_{a2} from the maximum temperature drops.

To obtain CD uniformity for a warped wafer, setpoint adjustments were made in real-time once warpage was detected. Warpage differed from wafer to wafer and hence not expected to be repeatable. If warpage was repeatable then we could have fixed but different bake-plate setpoints for center and edge.

For processing of Warp Wafer 10, the maximum temperature drop of 1.54°C and 1.70°C center and edge respectively were first measured. A search through Figures 7 and 8 gave $l_{a1} = 184\mu$m and $l_{a2} = 110\mu$m. Substitute into R_{a1}, R_{a2} and with the desired wafer temperatures of $T_{w1}(\infty) + T_a = 128.2$°C and $T_{w2}(\infty) + T_a = 126.6$°C, Equations (7) to (8) gave the new setpoints of $T_{p1}(\infty) + T_a = 133.6$°C and $T_{p2}(\infty) + T_a = 129.6$°C. Notice in Figure 9 the bake-plate setpoints were changed from 130°C to 133.6°C and 128.5°C to 129.6°C at $t = 24$s, immediately after the maximum bake-plate temperature drops had occurred. CD non-uniformity of 1 nm and wafer temperatures of 128.2°C (center) and 126.6°C (edge) were

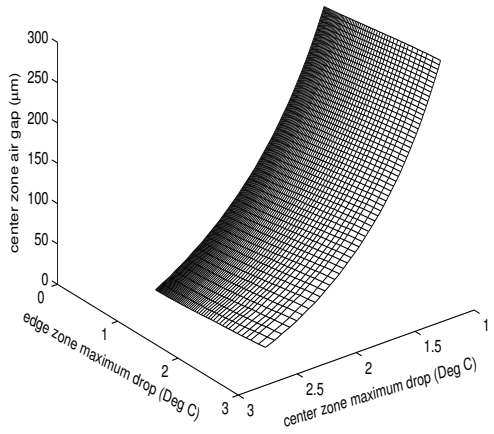

Fig. 7. Center-zone average air-gap versus bake-plate maximum temperature drops

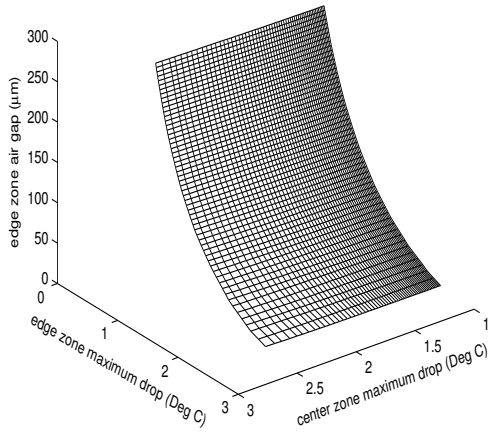

Fig. 8. Edge-zone average air-gap versus bake-plate maximum temperature drops

obtained, just like Flat Wafer 7. Note that $l_{a1} - l_{a2} = 74\mu$m $\neq 140\mu$m the center-to-edge warpage of Wafer 10 because l_{a1} and l_{a2} were not the air-gaps at the wafer center and extreme edge but the average over the center-zone and edge-zone.

4. CONCLUSION

The experimental results on CD control for a warped wafer are presented. To obtain CD uniformity for a warped wafer, bake-plate setpoints adjustments were made in real-time and on-line once warpage was detected and this could result in nonuniform temperature distribution across the wafer. For a wafer warped 140μm center-to-edge, CD nonuniformity was reduced to 1 nm.

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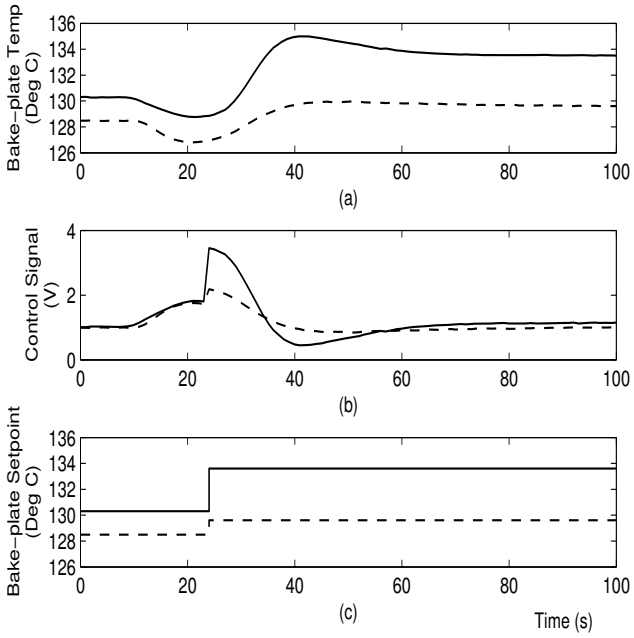

Fig. 9. Bake-plate setpoints adjusted in real-time once warpage was detected to give uniform CD for Warped Wafer 10. Solid-line: center, Dashed-line: edge

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