ROBUST DECENTRALIZED CONTROL OF A HVDC SYSTEM USING AN LMI APPROACH

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Abstract: A procedure for the design and tuning of two control loops of a High Voltage DC system is presented. The controlled variables are direct current on the rectifier side and direct voltage on the inverter side. The dynamics of both control loops interact with each other and are determined by the overall properties of the combined AC/DC system. Constraints on the information available for feedback in each loop require a decentralized controller structure. The AC system impedance is determined by the transmission lines, generators and loads and can suddenly change significantly, so the designed controllers must be robust against these variations. An LMI based iterative approach - referred to as PK-Iteration - is demonstrated to be an efficient tool for the design and tuning of such a decentralized control system. Moreover, even though the plant is of high dynamic order, the design procedure can be used to construct a low order controller.

Keywords: Robust Control, Iterative method, Linear matrix Inequalities, Decentralized control.

1. INTRODUCTION

This paper presents a procedure for the design and tuning of two coupled control loops in a High Voltage DC transmission link using a PK-iteration technique. In the case of long transmission lines or cables, only local information is available for feedback control on each side of the link. In practice, the two controllers are usually tuned manually as lead-lag compensators using classical frequency response methods. This is a time-consuming iterative trial-and-error procedure due to the dynamic interaction between the two sides. Automated design and tuning procedures are desirable because they result in faster project execution and lower engineering costs for tender and contract customization.

Two features that make it difficult to employ modern optimal and robust control techniques for a systematic design procedure are the above mentioned constraint that only local information is available, and the high dynamic order of the physical plant model. The latter results in controllers of high order. One way to overcome this problem is to use model or controller order reduction techniques, but this again leads to a trial and error procedure, since a controller that meets the design requirements with a low order model, is not guaranteed to meet any of them with a higher order model. The constraint on the use of information in a multi-variable controller leads to the problem of decentralized feedback control. The optimal solution to this problem is known to be difficult and in general requires solving an infinite dimensional optimization problem (Sourlas and

Manousiouthakis 1995). An approach often used in practice is a sequential design of decentralized control, see e.g. Hovd and Skogestad (Hovd and Skogestad 1994). But this again is an iterative procedure and not an automated tool for designing robust decentralized controllers.

The approach taken in this paper is first to reformulate the dynamic output feedback problem as a static output feedback problem by augmenting the plant model. This reformulation facilitates the iterative design of controllers with structural constraints. However, on its own it does not help much since stabilization by static output feedback is known to be a difficult and open problem. During recent years many ideas have been developed to tackle this problem, see for example (Beran and Karolos 1996),(Iwasaki 1999). In (Iwasaki 1999), a heuristic approach referred to as *dual iteration algorithm* and based on Linear Matrix Inequalities (LMI) was proposed. The efficiency of this new algorithm was demonstrated by extensive numerical examples. The algorithm does not allow the controller structure to be decentralized, but is very efficient for constructing stabilizing low order controllers. Here we will use the dual iteration algorithm for initializing an LMI based algorithm that allows to impose a decentralized structure on the controller.

Finally, robustness against model uncertainty is achieved using the small gain theorem by minimizing the H_∞ norm of a closed loop transfer function. The problem is formulated as a Bilinear Matrix Inequality (BMI) and solved using an iterative approach similar to that proposed by El Ghaoui and Balakrishnan (**?**).

This paper is organized as follows. Section 2 gives a brief description of HVDC systems and the control problem considered here. The controller design approach is described in section 3, and an iterative technique for solving the design problem is presented in section 4. Simulation results are shown in section 5, and conclusions are drawn in section 6.

2. HIGH VOLTAGE DC SYSTEMS

High Voltage Direct Current (HVDC) systems are used in electrical power grids as a supplement to AC transmission. Power transfer by means of HVDC is used in case of (i) interconnecting asynchronous AC systems with different power frequencies, (ii) high voltage cables longer than about 30-80km and (iii) long overhead lines with lengths in excess of about 600km (Kundur 1994). The system comprises two AC/DC power electronic converters separated by an equivalent impedance (Z_{DC}). On the AC side there are AC filters, while the AC grids can be represented by an equivalent impedance (Z_{AC}), as shown in Figure 1.

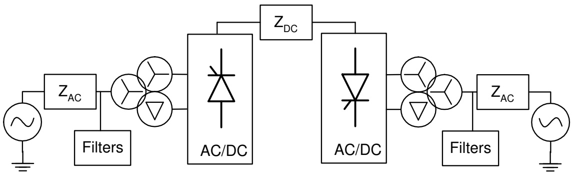

Fig. 1. High Voltage DC scheme

A state space model for this plant is proposed in (Aten *et al.* 2001); its high dynamic order (35 state variables) reflects the large number of passive elements. This model has been linearised for nominal AC voltages (1pu) and nominal firing angles (rectifier firing angle $\alpha = 21^o$, inverter extinction angle $\gamma = 25.6^o$) and extensively validated against nonlinear EMTDC simulation for small changes. The uncertain time delays due to the firing of the valves are ignored, since they are small relative to the control bandwidth, which is typically up to about 30Hz. As a result of the AC/DC interactions, the linearised model has zeros in the right half plane.

The DC side impedance is determined by the properties of a transmission line or cable, if present. In the case of a back-to-back scheme, where the two converters are physically close, the DC side impedance is just a conductor. The equivalent inductance of the converter transformers is modelled within the DC impedance. For a given HVDC scheme the DC impedance is normally accurately known, however this is not the case with the AC system impedance. The latter is determined by the transmission lines, generators and loads present at a certain time. In relation to this the Short Circuit Ratio (SCR) is defined as the ratio between Short Circuit Level ($V^2/|Z_{AC}|$) and the DC power transmitted (Kundur 1994). This parameter is uncertain within specified bounds and can suddenly change significantly when, for example, a transmission line is switched out to clear a fault.

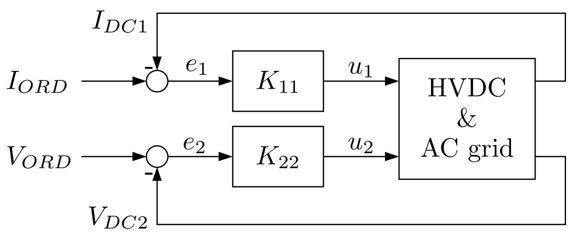

Fig. 2. Control configuration for HVDC transmission link

The control configuration is shown in Figure 2. Controlled variables are the direct current I_{DC1} on the rectifier side, and the direct voltage V_{DC2}

on the inverter side. These variables are also measured and available for feedback, but subject to the constraint that on the rectifier side only current measurements and on the inverter side only voltage measurements are used. The output vector

$$y = \begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} I_{DC1} \\ V_{DC2} \end{bmatrix}$$

is introduced and should track the reference input

$$r = \begin{bmatrix} r_1 \\ r_2 \end{bmatrix} = \begin{bmatrix} I_{ORD} \\ V_{ORD} \end{bmatrix}$$

Control inputs are u_1 (ϵ_1, the input controlling the phase-locked oscillator on side 1) and u_2 (ϵ_2 on side 2). On each side the inputs u_1 and u_2 are passed to phase locked oscillators, which send firing pulses to the thyristor valves in the converter bridges. The resulting firing angles determine the amount of direct voltage and direct current flowing through the link.

It is difficult to continuously measure the short circuit ratios (SCR1 on the rectifier side and SCR2 on the inverter side), therefore these parameters must be treated as uncertain within given bounds. The admissible range for the short circuit ratios on both sides is $2.0 \leq$ SCR1, SCR2 ≤ 9.0. Varying both parameters independently in steps of 1 leads to 64 different operating conditions.

The phase-locked oscillators act as integrators in the control loop. Even though the decentralized controller structure imposes a constraint, it facilitates the design on the other hand because together with the integral action of the phase-locked oscillator on each side it helps to achieve zero steady-state error after step changes.

Table 1. Performance and robustness requirements

Settling time	$\leq 200msec$
Peak overshoot ($u_1 \to y_1$), ($u_2 \to y_2$)	$\leq 25\%$
Cross perturb. ($u_1 \to y_2$), ($u_2 \to y_1$)	$\leq 50\%$
Robust stability	$2 \leq SCR1 \leq 9$
	$2 \leq SCR2 \leq 9$

The dynamics of both control loops interact with each other and are determined by the overall properties of the combined AC/DC system. It is common practice to design the inner control loops for HVDC sequentially by trial and error, using classical methods. Applications of modern control techniques have been reported recently. H_∞ controller design was used on the inverter side only in (Jovcic *et al.* 1999). Genetic algorithms have been proposed for the design of a PID controller for a HVDC system in (Farag *et al.* 2002), (Wang *et al.* 2000), where a regulator problem is considered.

For step changes in the set points of I_{DC1} or V_{DC2}, the set of performance and robustness requirements is given in Table 2.

3. CONTROLLER DESIGN

Let a family of linear state space models that capture the dynamics of the HVDC system over all admissible operating conditions be given by

$$\begin{aligned} \dot{x} &= A_i x + Bu, \quad i = 1, 2, ..., N \\ y &= Cx \end{aligned} \tag{1}$$

where $x \in \mathbb{R}^n$ is the state vector, $u \in \mathbb{R}^{n_i}$ is the input vector, $y \in \mathbb{R}^{n_o}$ is the output vector, $A_i \in \mathbb{R}^{n \times n}$, $B \in \mathbb{R}^{n \times n_i}$, and $C \in \mathbb{R}^{n_o \times n}$. Note that the matrix A_i denotes the value of A at the operating condition i. The input and output matrices B and C are not affected by the short circuit ratios.

For the purpose of the controller design, the uncertainty of the model (1) is expressed in the form of a generalized plant P with state space realization

$$\begin{aligned} \dot{x} &= A_0 x + B_1 w_1 + Bu \\ z_1 &= C_1 x \\ y &= Cx \end{aligned} \tag{2}$$

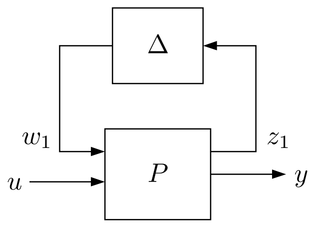

Fig. 3. Generalized plant

The generalized plant P is shown in Figure 3. The physical plant model (1) is represented by the matrices (A_0, B, C), where A_0 stands for the nominal value of the uncertain matrices A_i. Perturbations of the nominal plant matrix A_0 are expressed via fictitious inputs through B_1, fictitious outputs through C_1 and a fictitious feedback loop $w_1 = \Delta z_1$, where Δ is a real gain matrix, such that all the operating conditions are covered, in the sense that for each operating condition there exists a Δ_i such that

$$(A_0 + B_1 \Delta_i C_1) = A_i, , \quad \|\Delta_i\| < 1, \quad i = 1, 2, .., 64 \tag{3}$$

A systematic method of constructing B_1, C_1 such that $\|\Delta\| < 1$ tightly covers all admissible operating conditions is given in (Werner *et al.* 2003) and has been used here.

Based on the small gain theorem, the robust stability of the system (2) is guaranteed upon finding a feedback controller $K(s)$ from y to u with state space realization

$$\dot{\zeta}(t) = A_K\zeta(t) + B_K y(t)$$
$$u(t) = C_K\zeta(t) + D_K y(t) \quad (4)$$

such that the closed-loop transfer function satisfies $\|T(s)_{z_1w_1}\|_\infty < 1$, where $A_k \in \mathbb{R}^{n_c\times n_c}$, $B_K \in \mathbb{R}^{n_c\times n_o}$, $C_K \in \mathbb{R}^{n_i\times n_c}$, $D_K \in \mathbb{R}^{n_i\times n_o}$, $n_c \le n$ is the order of the controller. It is well known that this problem can be reformulated as a static output feedback problem by introducing the augmented system

$$\hat{A}_0 = \begin{bmatrix} A_0 & 0 \\ 0 & 0_{n_c} \end{bmatrix}, \hat{B} = \begin{bmatrix} B & 0 \\ 0 & I_{n_c} \end{bmatrix}, \hat{C} = \begin{bmatrix} C & 0 \\ 0 & I_{n_c} \end{bmatrix}$$
$$\hat{B}_1 = \begin{bmatrix} B_1 \\ 0 \end{bmatrix}, \hat{C}_1 = \begin{bmatrix} C_1 & 0 \end{bmatrix}$$

It is straight forward to show that static output feedback control $u = \hat{K}y$, where

$$\hat{K} = \begin{bmatrix} D_k & C_k \\ B_k & A_k \end{bmatrix} \in R^{(n_i+n_c)\times(n_o+n_c)} \quad (5)$$

applied to the augmented system

$$\begin{aligned} \dot{x} &= \hat{A}_0 x + \hat{B}_1 w_1 + \hat{B}u \\ z_1 &= \hat{C}_1 x + \hat{D}_1 u \\ y &= \hat{C}x \end{aligned} \quad (6)$$

leads to the same closed-loop system as the controller (4) applied to (2). Thus, instead of designing a dynamic controller of order n_c for the system (2) we can design a static output feedback controller for the system (6).

To enforce a decentralized controller structure, the constraint $\hat{K} \in \mathcal{K}_s$, where

$$\mathcal{K}_s = \{\hat{K} \in R^{(n_i+n_c)\times(n_o+n_c)} : \ A_K,\ B_K,\ C_K,\ D_K \text{ are all diagonal}\} \quad (7)$$

is imposed.

To satisfy the settling time requirement, the closed loop poles will be pushed as far as possible to the left of the complex plane. The design problem can thus be formulated as

$$\min_{\hat{K}\in\mathcal{K}_s} \rho(\hat{A}_0 + \hat{B}\hat{K}\hat{C}) \quad \text{subject to} \quad \|T_{z_1w_1}\|_\infty < \gamma_B \quad (8)$$

where $\kappa(\cdot)$ denotes the maximum real part of the eigenvalues of a matrix, and γ_B is a tuning parameter that can be used to trade robustness of the closed system against performance. Using the real bounded lemma (Boyd *et al.* 1994) the above problem can be reformulated as

$$\min_{\hat{K}\in\mathcal{K}_s} \kappa(\hat{A}_0 + \hat{B}\hat{K}\hat{C}) \quad \text{s.t.} \quad \Phi(P,\hat{K},\gamma) < 0,\ P > 0 \quad (9)$$

where

$$\Phi(P,\hat{K},\gamma) = \begin{bmatrix} \hat{A}_0P + \hat{B}\hat{K}\hat{C}P + (*) & \hat{B}_1 & P\hat{C}^T \\ \hat{B}_1^T & -\gamma I & 0 \\ \hat{C}_1P & 0 & -\gamma I \end{bmatrix} \quad (10)$$

and $(*)$ denotes a term required to make the matrix symmetric.

Note that the first constraint in (9) is bilinear in P and $\hat{K}$. In the next section an iterative algorithm for solving this problem, based on solving a sequence of LMI problems, is presented.

4. PK-ITERATION ALGORITHM

The design problem is solved in three stages: starting with a controller of order n_c that stabilizes the nominal system, in the first stage a stabilizing decentralized controller is constructed. In the second stage, robustness is achieved by minimizing a H_∞ norm, and in stage three the speed of response is maximized.

Define left and right multipliers N_L and N_R for $\hat{K}$ such that the product $N_L\hat{K}N_R$ enforces the required block diagonal structure of A_K, C_K, C_K, D_K.

Let $\varepsilon > 0$ be a scalar, and define

$$\Psi(\hat{K},\varepsilon) = \begin{bmatrix} \varepsilon I & N_L\hat{K}N_R \\ N_R^T\hat{K}^TN_L^T & I \end{bmatrix} \quad (11)$$

It is clear that if $\Phi(\hat{K},\varepsilon) > 0$ holds then $\varepsilon > \|N_L\hat{K}N_R\|^2$, thus ε is an upper bound on the norm of the off-diagonal controller terms.

With these definitions, the design procedure can be summarized as follows.

Design procedure (PK-Iteration)

0) *Use the dual iteration procedure described below to find a controller of order n_c that stabilizes the nominal plant model, and construct $\hat{K}$.*
1) *Squeeze off-diagonal terms of $\hat{K}$ by minimizing ε: repeat*
   P-step Set $\hat{K}_m = \hat{K}$, solve
   $$\max_{P>0} \theta \quad : \quad I\theta + \Phi(P,\hat{K}_m,\gamma) < 0$$
   where $\theta > 0$ is scalar
   K-step Set $P_m = P$, solve
   $$\min_{\hat{K}} \varepsilon \ : \ \Phi(P_m,\hat{K},\gamma) < 0\,, \ \ \Psi(\hat{K},\varepsilon) > 0$$
   until $\varepsilon < \varepsilon_B$ (a small positive constant).
2) *Achieve the prescribed degree of robustness by minimizing γ: repeat*

P-step Set $\hat{K}_m = \hat{K}$, solve

$$\min_{P>0} \gamma \quad : \quad \Phi(P, \hat{K}_m, \gamma) < 0$$

K-step Set $P_m = P$, solve

$$\min_{\hat{K}} \gamma \ : \ \Phi(P_m, \hat{K}, \gamma) < 0, \ \Psi(\hat{K}_m, \varepsilon_B) > 0$$

until $\gamma < \gamma_B$.

3) *Get the best possible performance by replacing A_0 by $A_0 + \alpha I$*, where $\alpha > 0$ is a sufficiently small scalar: repeat

P-step Set $\hat{K}_m = \hat{K}$, solve

$$\max_{P>0} \theta \quad : \quad I\theta + \Phi(P, \hat{K}_m, \gamma_B) < 0\,, \ \ P > 0$$

K-step Set $P_m = P$, solve

$$\max_{\hat{K}} \theta : I\theta + \Phi(P_m, \hat{K}, \gamma_B) < 0, \Psi(\hat{K}_m, \varepsilon_B) > 0$$

Increase α and go to P-step, until a specified performance limit is reached or no feasible solution is obtained.

The above algorithm requires an initial fixed order stabilizing controller. For this purpose the dual iteration procedure proposed in (Iwasaki 1999) can be used, which is briefly summarized here.

Initialization: Dual Iteration Procedure

Introduce matrices $G \in \mathbb{R}^{n_i \times (n+n_c)}$, $F \in \mathbb{R}^{(n+n_c)\times n_o}$, $X = X^T \in \mathbb{R}^{(n+n_c)\times(n+n_c)}$, $Y = Y^T \in \mathbb{R}^{(n+n_c)\times(n+n_c)}$, and let μ be a scalar.

(1) Choose an arbitrary initial value G_o for G and set k=1.

(2) Fix $G = G_{k-1}$ and solve

$$\hat{\mu}_k := \min_{Y>0} \mu : \begin{cases} Y(\hat{A} + \hat{B}G) + (\hat{A} + \hat{B}G)^T Y < \mu Y \\ \hat{C}^{T\perp}(Y\hat{A} + \hat{A}^T Y - \mu Y)\hat{C}^{T\perp T} < 0 \end{cases}$$

Let $F_k = -\sigma Y^{-1}\hat{C}^T$, for sufficiently large $\sigma > 0$.

(3) Fix $F = F_k$ and solve

$$\mu_k := \min_{X>0} \mu : \begin{cases} \hat{B}^{\perp}(\hat{A}X + X\hat{A}^T - \mu X)\hat{B}^{\perp T} < 0 \\ (\hat{A} + F\hat{C})X + X(\hat{A} + F\hat{C})^T < \mu X \end{cases}$$

Let $G_k = -\sigma B^T X^{-1}$, for sufficiently large $\sigma > 0$.

(4) If $\mu_k < 0$, then stop. Otherwise let k=k+1 and go to step 2.

Once the above algorithm has converged to a negative value for μ and some $X > 0$, lemma 1 in (Iwasaki 1999) guarantees the existence of $\hat{K}$ that satisfies the LMI

$$(\hat{A} + \hat{B}\hat{K}\hat{C})X + X(\hat{A} + \hat{B}\hat{K}\hat{C})^T < \mu X$$

Now, selecting $P = X$ guarantees the existence of $\hat{K}$ such that $\Phi(P, \hat{K}, \gamma) < 0$ is satisfied for a sufficiently large γ.

Observations

- The PK iteration design procedure consists of solving a sequence of LMI problems, for which efficient LMI solvers are available.
- When there is no specified objective to be minimized (i.e. γ or ε), a slack variable θ is introduced and used to maximize the feasibility of the problem over the free variable P or $\hat{K}$.
- The global convergence of the above algorithm is not guaranteed, but the cost is monotonically improving (i.e. ε-decreasing, γ-decreasing and α-increasing).

5. RESULTS AND SIMULATION

In this section the design procedure given in the previous section is applied to design a low-order decentralized controller for the HVDC system. Applying the dual iteration procedure with $n_c = 2$ the following controller is obtained in just two iterations

$$K_1(s) = \begin{bmatrix} \frac{3.5(s + 2.2\cdot10^6)(s - 157.8)}{(s + 10^7)(s + 2093)} & \frac{-9.78(s + 1.5\cdot10^6)(s - 1.3)}{(s + 10^7)(s + 2093)} \\ \frac{3.5(s + 2.2\cdot10^6)(s - 157.8)}{(s + 10^7)(s + 2093)} & \frac{9.1(s + 1.4\cdot10^6)(s + 64.6)}{(s + 10^7)(s + 2093)} \end{bmatrix}$$

The controller K_1 stabilizes the nominal system (6). Now applying stage 1 of the design procedure leads to

$$K_2(s) = \begin{bmatrix} \frac{-3.9\cdot10^{-3}s - 0.0145}{s + 3.873} & 0 \\ 0 & \frac{5.5\cdot10^{-4}s + 3.3\cdot10^{-3}}{s + 4.225} \end{bmatrix}$$

This controller is decentralized but is not robust ($\gamma \approx 3.5$). Applying stage 2 of the design procedure yields

$$K_3(s) = \begin{bmatrix} \frac{-7.5\cdot10^{-3}s - 0.057}{s + 16.32} & 0 \\ 0 & \frac{5.7\cdot10^{-4}s + 3.468\cdot10^{-4}}{s + 4.576} \end{bmatrix}$$

Controller K_3 is decentralized and satisfies $\gamma < 1.5$ with $\kappa(\bar{A}) = -0.118$, where $\bar{A}$ is the closed-loop state matrix. Finally applying stage 3 of the design procedure leads to:

$$K(s) = \begin{bmatrix} \frac{-0.091s - 0.789}{s + 8.65} & 0 \\ 0 & \frac{0.068s + 0.362}{s + 6.56} \end{bmatrix}$$

This controller is decentralized and satisfies $\gamma < 1.5$ with $\kappa(\bar{A}) = -6.47$. The convergence of the PK-iteration algorithm is shown in Figure 4.

The response of the closed-loop system to step changes in the set points for I_{DC1} and V_{DC2} at different operating conditions is shown in Figure 5.

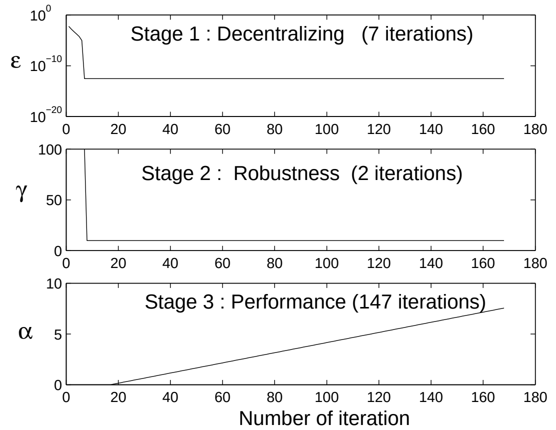

Fig. 4. Convergence of the stages of PK-ietration

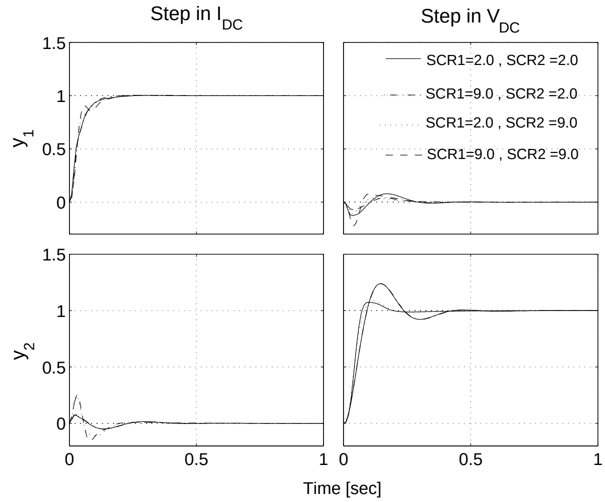

Fig. 5. Simulated step responses of the HVDC model

6. CONCLUSION

This paper considers the problem of designing a robust, decentralized low order controller for a HVDC system. A practical procedure that allows successful implementation of modern robust control tools for such a problem has been presented. The design procedure is computationally efficient since it involves only the solution of LMI problems, for which efficient solvers are available. Although - similar to DK iteration for the structured singular value μ - the global convergence of the proposed techniques is not guaranteed, experience suggests that it converges quite well in most cases. The semi-automated procedure presented here can serve as a template for many similar design problems that involve structural constraints on the controller.

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