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ROBUST CONTROL DESIGN FOR PARALLELED DC/DC CONVERTERS WITH CURRENT SHARING

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Abstract: This paper concerns a robust control design for multi-loop operation of paralleled DC/DC converters in the presence of uncertainties. The system is composed of voltage-loop and current-loop subsystems. The PID controller is firstly designed to achieve the robust stability and robust performance of the voltage-loop. Then, the PI controller for the current-loop is designed to achieve the robust stability and robust performance of the overall system. The μ-analysis is used to evaluate the robustness of both controllers. Simulation results are presented to demonstrate the control design procedure. *Copyright © 2002 IFAC*

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1. INTRODUCTION

Current sharing among converters is the main control issue in parallel-connected converters. The common reasons for paralleling power converters are either to increase the power output capability above the rating of a single module or to provide for redundancy so that a single module failure will not affect the system operation. Paralleling power converters adds complexity to the system and typically entails accepting some performance and cost compromises. In practice, the control is needed to ensure proper current sharing and many effective control schemes have been proposed in previous studies, such as (Choi, 1998), (Garabandic and Petrovic, 1995), (Perreault, *et al*., 1999), and (Thottuvelil and Verghese, 1998). One common approach is to employ an active control scheme to force the currents in parallel converters to follow the reference current, which is an average current of converters. Such a scheme is commonly known as the democratic current sharing scheme as presented in (Jovanovic, *et al*., 1996), and (Siri et al. 1992). Also if the reference current is the output current of one converter, such a scheme is known as the master-slave current sharing as presented in (Panov, *et al*., 1997), (Rajagopalan, *et al*., 1996), and (Siri, *et al*., 1992). The essence of an active control is to monitor the difference between the reference current and the output current of each converter and incorporate this information into the control of voltage-loop. The necessity of reliable control system that offers robust stability for the overall system and robust performance for its dynamics in the presence of uncertainties is recommended, as presented in (Buso, 1999), (Garabandic and Petrovic, 1995), and (Tymerski, 1996). However a single module has only been considered. The procedure of designing a robust controller requires a model that takes the uncertainties of the system into consideration, as studied in (Skogestad and Postlethwaite, 1997). The main purpose of this paper is to design a practical robust control of paralleled DC/DC converters, as shown in Fig. 1. The overall system is composed of two-MIMO subsystems, for voltage-loop and current-loop. The voltage-loop consists of *n*-SISO subsystems, where *n* is the number of converters in parallel that can be designed separately. The actual plant models consist of nominal plant models and uncertainty models. Parametric uncertainty is modeled where the structure of the model is known, but some of the parameters are uncertain. Robust PID and PI controllers are proposed to achieve robust stability and robust performance for voltage-loop and

current-loop, respectively. The control design procedure presented is verified by simulation of two 500W-buck converters connected in parallel. However it can be extended to a real system of *n*-units in parallel.

2. SYSTEM DESCRIPTIONS AND UNCERTAINTY

Consider the state-space representation of averaged and linearized model that is presented in (Gadoura, *et al*., 2001), the transfer matrix of the system can be written as follows.

$$y = G_p\, u + G_d\, d \tag{1}$$

where y is the vector of output voltages and output currents, G_p is the plant model transfer matrix, u is the control commands vector, G_d is the disturbance model transfer matrix, and d is the disturbances vector. For simplicity the system can be split to two subsystems, one for voltage-loop and another for current loop.

$$\begin{bmatrix} y_v \\ --- \\ y_i \end{bmatrix} = \begin{bmatrix} G_{pv} \\ --- \\ G_{pi} \end{bmatrix} u + \begin{bmatrix} G_{dv} \\ --- \\ G_{di} \end{bmatrix} d \tag{2}$$

where the subscript "*v*" stands for voltage-loop subsystem and "*i*" for current-loop subsystem. The voltage-loop subsystem can be composed of *n*-loops of SISO subsystems that help to design each voltage-loop of each converter separately.

$$y_{v_j} = G_{p_{v_j}}\, u_j + G_{d_{v_j}}\, d_j \tag{3}$$

where $j = 1, 2, \ldots, n$.
The voltage-loop design problem is illustrated in Fig. 2 when the disconnection at point "*a*" occurs. The design objective is to determine the controller parameters so that the system is robust with respect to changes in the line and load disturbances as well as in the plant model.

2.1. Controller Structure

From Fig. 1, the control system of one converter is a voltage controller (k_{vj}) ensuring robust output voltage cascaded with current controller (k_j) ensuring current sharing.

$$\begin{aligned} u_j &= k_{v_j} k_j\, e_{i_j} + k_{v_j}\, e_{v_j} \\ &= k_{i_j}\, e_{i_j} + k_{v_j}\, e_{v_j} \end{aligned} \tag{4}$$

From the practical viewpoint, the controllers' structure of either voltage-loop or current-loop can be presented as a diagonal transfer matrix.

$$K_v = \mathrm{diag}\left(k_{v_1}, k_{v_2}, \cdots, k_{v_n}\right) \tag{5}$$

$$K_i = \mathrm{diag}\left(k_{i_1}, k_{i_2}, \cdots, k_{i_n}\right) \tag{6}$$

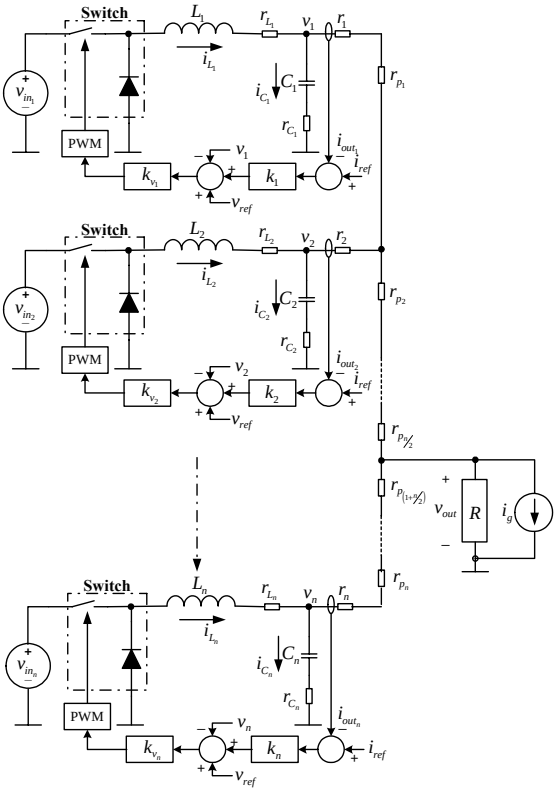

Fig. 1. Paralleled DC/DC converters feeding a resistive load with cascaded controllers for voltage- and current-loops.

where K_v and K_i are used in control design procedure as shown in Fig. 2. Then, the control vector can be written in the general form as follows.

$$u = K_i\, e_i + K_v\, e_v \tag{7}$$

where e_i is a vector of current error and e_v is a vector of voltage error. Note that Q block in Fig. 2 determines the active control scheme either democratic or master-slave scheme.

$$Q_{m-s} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 \\ 1 & -1 & 0 & \cdots & 0 \\ 1 & 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & -1 \end{bmatrix} \text{ and } Q_d = \begin{bmatrix} \frac{1-n}{n} & \frac{1}{n} & \cdots & \frac{1}{n} \\ \frac{1}{n} & \frac{1-n}{n} & \cdots & \frac{1}{n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{1}{n} & \frac{1}{n} & \cdots & \frac{1-n}{n} \end{bmatrix}$$

where $Q_{m\text{-}s}$ is for master-slave scheme $\left(i_{ref} = i_{out_1}\right)$ and Q_d is for democratic scheme.

2.2. Uncertainty Model

A general procedure to handle the parametric uncertainty is presented in many literature (Skogestad and Postlethwaite, 1997) and (Tymerski, 1996). Consider the perturbed plant models of equation (2) as shown in Fig. 2.

$$\tilde{G}_{p_v} = \tilde{C}_{p_v}\left(sI - \tilde{A}_p\right)^{-1} \tilde{B}_p \text{ (for voltage-loop)} \tag{8}$$

$$\tilde{G}_{p_i} = \tilde{C}_{p_i}\left(sI - \tilde{A}_{p_i}\right)^{-1} \tilde{B}_{p_i} \text{ (for current-loop)} \tag{9}$$

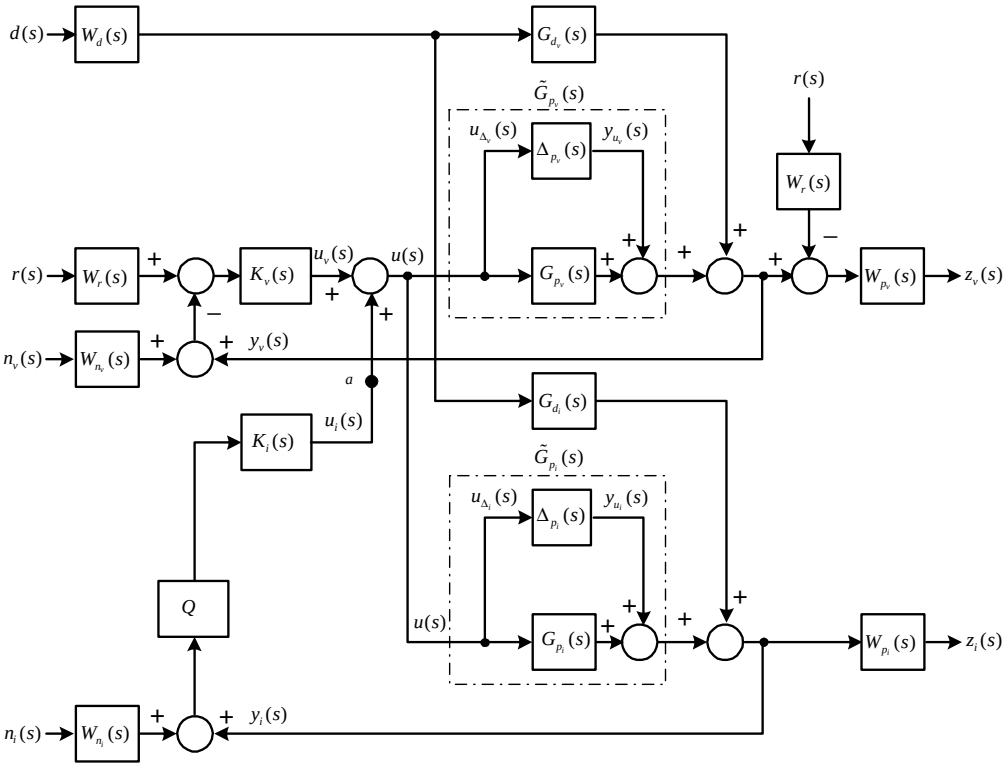

Fig. 2. The control configuration of paralleled DC/DC converters including all uncertainties. The control of voltage-loop is considered when it is isolated from the current-loop by breaking the connection at point *a*.

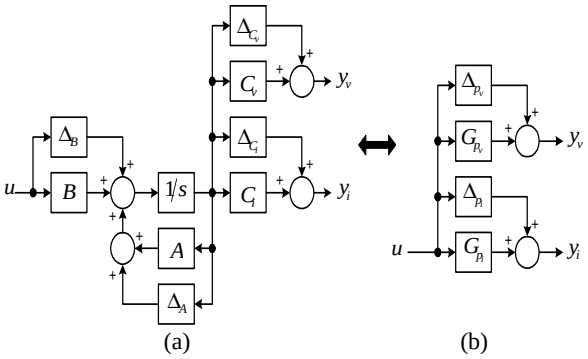

Fig. 3. The parametric uncertainty in state-space representation and its equivalent that inserts into the control system of Fig. 2.

These transfer matrices can be presented as a perturbed state-space model as follows.

$$\begin{aligned} \dot{x} &= \tilde{A}_p x + \tilde{B}_p u \\ y_v &= \tilde{C}_{p_v} x \quad \text{and} \quad y_i = \tilde{C}_{p_i} x \end{aligned} \tag{10}$$

The perturbed state-space matrices can be realized as shown in Fig. 3(a), where Fig. 3(b) shows how to adapt the uncertainty model into Fig. 2.

$$\tilde{A}_p = A_p + \Delta_A,\ \tilde{B}_p = B_p + \Delta_B, \text{ and}$$
$$\tilde{C}_{p_{v(or\,i)}} = C_{p_{v(or\,i)}} + \Delta_{C_{v(or\,i)}}$$

where A_p, B_p, and C_{pv} model the nominal system, however Δ_A, Δ_B, and Δ_C model the uncertainty, *i.e. the real parameters' variations in power components of converters.* The uncertain perturbations are chosen into a block-diagonal matrix as follows.

$$\Delta_{p_v} = \text{diag}\left(\Delta_A, \Delta_B, \Delta_{C_v}\right) \tag{11}$$
$$\Delta_{p_i} = \text{diag}\left(\Delta_A, \Delta_B, \Delta_{C_i}\right) \tag{12}$$

3. ROBUST CONTROL

Here we will design and analyze the robust control of the closed-loop system in Fig. 5, however the same procedure has been applied to the closed-loop system in Fig 4, *i.e. voltage-loop design*. From Fig. 5(a), P is the nominal system, K_v is the voltage-loop controller, K_i is the current-loop controller, and the Δ is the uncertainty.

$$\Delta \in \mathbf{\Delta} \equiv \left\{\Delta : \Delta = \text{diag}\left\{\Delta_{p_v}, \Delta_{p_i}\right\}, \|\Delta\|_\infty \le 1\right\} \tag{13}$$

Using upper linear fractional transformation (upper-LFT), the system may be represented as in Fig. 5(b), where G is the perturbed transfer matrix from w and u to z and y. This configuration is used to design the controller that stabilizes the system in the presence of uncertainty. The closed-loop transfer matrix from $\begin{bmatrix} v_\Delta & w \end{bmatrix}^T$ to $\begin{bmatrix} y_\Delta & z \end{bmatrix}^T$ can be written in the form of a lower LFT, which is used to analyze the system.

$$\begin{aligned} N &= F_l\left(P, K\right) = P_{11} + P_{12}K\left(I - P_{22}K\right)^{-1}P_{21} \\ &= \begin{bmatrix} N_{11} & N_{12} \\ N_{21} & N_{22} \end{bmatrix} \end{aligned} \tag{14}$$

where $v_\Delta = \begin{bmatrix} u_{\Delta_v} & u_{\Delta_i} \end{bmatrix}^T$, $w = \begin{bmatrix} r & d & n_v & n_i \end{bmatrix}^T$, $y_\Delta = \begin{bmatrix} y_{u_v} & y_{u_i} \end{bmatrix}^T$, and $z = \begin{bmatrix} z_v & z_i \end{bmatrix}^T$.

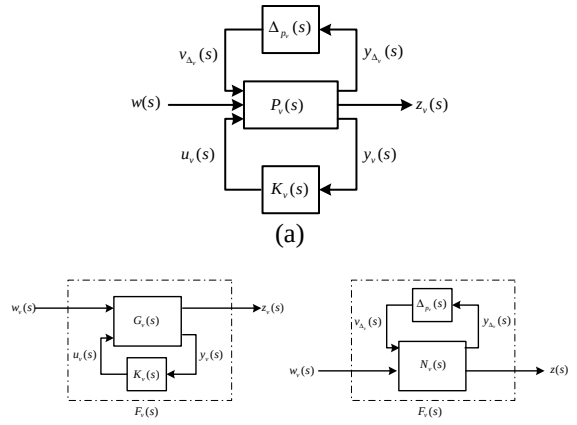

Fig. 4. The general configurations that considered to design and analysis the voltage-loop control of paralleled DC/DC converters in the presence of uncertainty.

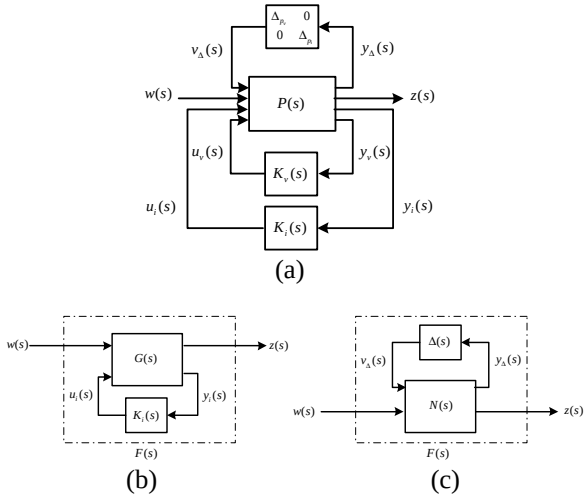

Fig. 5. The general configurations that considered to design and analysis the current-loop control of paralleled DC/DC converters in the presence of uncertainty.

To ensure good performance, we would like to have $\|N_{22}\|_\infty$ small. The uncertain closed-loop transfer matrix *F(s)* from *w* to *z* is obtained by using an upper LFT

$$F = F_u\left(N,\Delta\right) = N_{22} + N_{21}\Delta\left(I - N_{11}\Delta\right)^{-1} N_{12} \quad (15)$$

For robust stability, the system must remain stable for all plants in the uncertainty set. This should satisfy that *F(s)* is stable for all Δ where $\|\Delta\|_\infty \le 1$. Robust performance is achieved if the robust stability is satisfied and the transfer matrix from *w* to *z* is small for all plants in the uncertainty set.

$$\|F(s)\|_\infty < 1 \text{ for all } \Delta \text{ where } \|\Delta\|_\infty \le 1 \qquad (16)$$

4. CONTROL DESIGN

4.1. Voltage-loop Design

The PID controller has been chosen to regulate the voltage-loop in order to achieve the robust output voltage in spite of line and load disturbances.

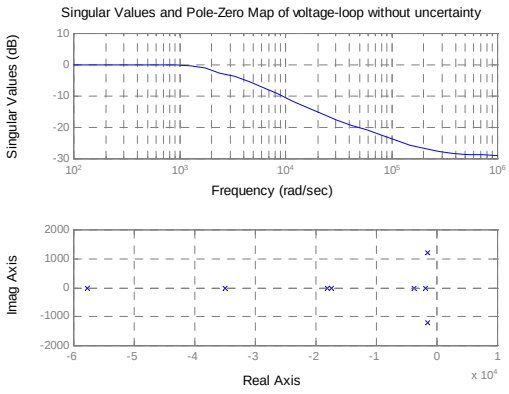

Fig. 6. The nominal performance and stability tests for voltage-loop, i.e. $\bar{\sigma}\left(N_{v_{11}}\right)<1$ for all ω and N_v has all poles in LHP.

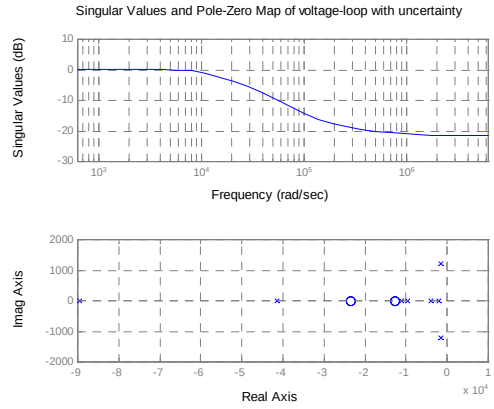

Fig. 7. The robust performance and stability tests for uncertain voltage-loop, i.e. $\bar{\sigma}\left(F_v\right)<1$ for all ω and F_v has all poles in LHP

Recalling equation (3) each voltage-loop of each converter can be designed separately, which means that the control design of one-buck converter, as presented explicitly in (Gadoura, *et al.*, 1999), can be utilized in this stage. As long as the paralleled buck converters are identical, the control design procedure of one buck converter can be duplicated for other converters. In general, a good literature of the tuning rules of PID controller are studied and discussed in (Astrom and Hagglund, 1995). The PID controllers are designed to achieve the robust stability and robust performance of the voltage-loop.

RS $\Leftrightarrow$ $F_v(s)$ is internally stable

RP $\Leftrightarrow$ $\|F_v(s)\|_\infty < 1$ for all Δ_v where $\|\Delta_v\|_\infty \le 1$

4.2. Current-loop Design

The PI controller, which is *k* in equation (4), has been selected to equalize the output current of each converter to the current reference. After designing the voltage-loop of each converter, the PI controllers are tuned to achieve the robust stability and robust performance of the overall system.

RS $\Leftrightarrow$ $F(s)$ is internally stable

RP $\Leftrightarrow$ $\|F(s)\|_\infty < \gamma$ for all Δ where $\|\Delta\|_\infty \le 1$

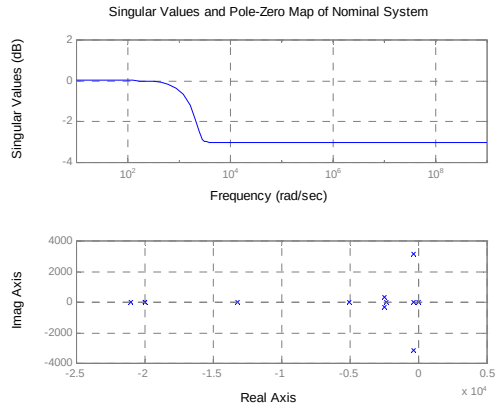

Fig. 8. The nominal performance and stability tests for the overall system, i.e. $\bar{\sigma}(N_{11}) < \gamma$ for all ω and N has all poles in LHP.

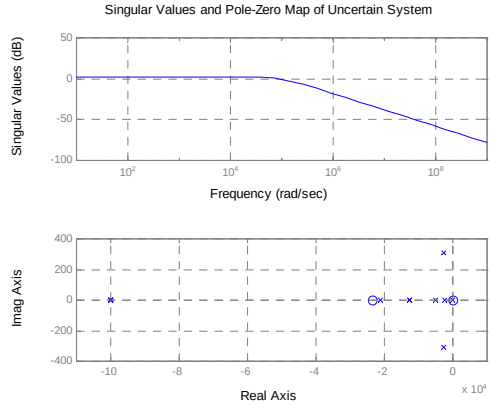

Fig. 9. The robust performance and stability tests for uncertain system, i.e. $\bar{\sigma}(F) < \gamma$ for all ω and F has all poles in LHP.

5. DESIGN EXAMPLE

The configuration of two-identical parallel-connected buck converters, as shown in Fig. 2, is considered to verify the control design procedure. The specifications are given as follows. The input voltage V_{in} = 140V, output voltage V_o = 54V, maximum output power P_o = 500W, switching frequency f_s = 100kHz, inductor L = 100μH, capacitor C = 1000μF, output resistance R = 11Ω, equivalent series resistor of capacitor r_C = 50mΩ, equivalent series resistor of inductor r_L = 15mΩ, interconnection resistance r_p = 0Ω, cable resistance r = 20mΩ. Also the controllers' parameters are identical for both converters and have the following parameters. PID-controller, K_p=22.665, T_i=0.745ms, T_d=0.169ms, N=4, and b=0.573. PI-controller, K_p=2 and T_i=0.2ms. The PI and PID controllers' structures are as follows, respectively.

$$u_{i_j} = K_{p_j}\left(1+\frac{1}{T_{i_j}s}\right)\left(i_{ref_j} - i_{out_j}\right) \qquad (17)$$

$$u_{v_j} = K_{p_j}\left(b_j\left(v_{ref_j}+u_{i_j}\right) - v_j + \frac{1}{T_{i_j}s}\left(v_{ref_j}+u_{i_j}-v_j\right) - \frac{T_{d_j}s}{T_{d_j}/N_j s+1}v_j\right) \qquad (18)$$

The high-pass filter matrices, $W_{nv}(s)$ and $W_{ni}(s)$, are designed to attenuate the measurement noise, which is ignored, i.e., $n_v = n_i = 0$, in the simulation. The low-pass filter matrices, $W_{pv}(s)$ and $W_{pi}(s)$, are designed to specify the desired closed-loop performance for the voltage-loop and the current-loop, respectively. Also they are implemented to reduce the ripples in the output currents and voltages in order to study the disturbance rejection capability of the system. Also $W_d(s)$ and $W_r(s)$ are scaling matrices. In Fig. 6, nominal performance (NP) and nominal stability (NS) of the voltage-loop are achieved where the maximum singular value is less than 1 and all the poles are located in LHP. Also the robust performance (RP) and robust stability (RS) of the voltage-loop are achieved as shown in Fig. 7. In Fig. 8 and Fig. 9, NP, NS, RP, and RS of the overall system are achieved where γ is equal to 1.27, which is violating the robust performance of the overall system. However the simulation results of the worst-case show that the system is robustly performed and stable as shown in Fig. 11 and Fig. 12. Note that few poles those are very large are not seen in the pole-zero maps because of figure scales.

6. CONCLUSION

The paper has presented a procedure to split the system of paralleled DC/DC converters to two subsystems, voltage-loop and current-loop. The voltage-loop consists of n subsystems that help to design each one separately. The PID controllers are designed to regulate the voltage-loop and to achieve the robust performance and robust stability in the presence of the uncertainty. The output voltages of uncertain and nominal two-buck converters in parallel are presented in Fig. 10. It shows that the voltage-loop design has good rejection ability of line and load disturbances in both cases. The PI controllers are designed to regulate the current-loop of the system where the outputs are injected into their voltage-loops. The PI controllers are succeeded to achieve the robust performance and robust stability of the current-loop. The output voltages and output currents of two paralleled buck converters in the presence of uncertainty are presented in Fig. 11 and Fig. 12, respectively. The overall system has good rejection ability of line and load disturbances with zero steady-state error, small peaks, and fast recovery time.

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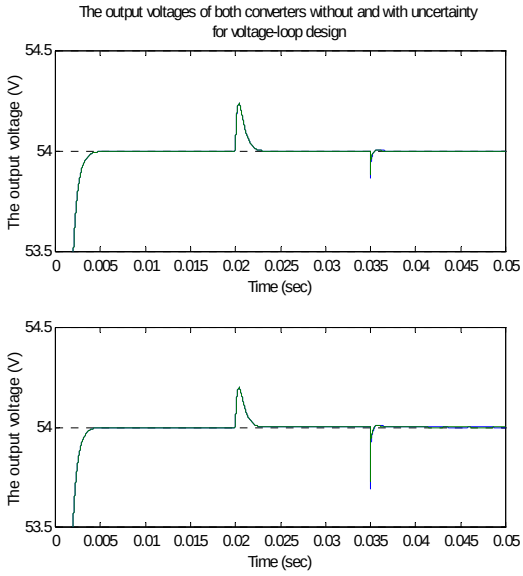

Fig. 10. The steady state and transient behavior of the output voltage of the voltage-loop in the presence of line & load disturbances without and with uncertainty, respectively.

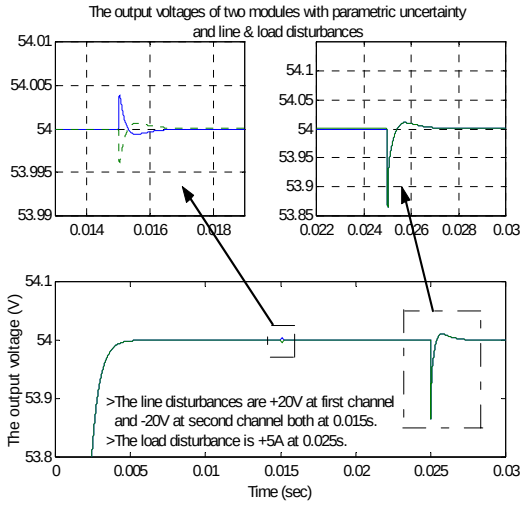

Fig. 11. The steady state and transient behavior of the output voltages in the presence of line & load disturbances with uncertainty.

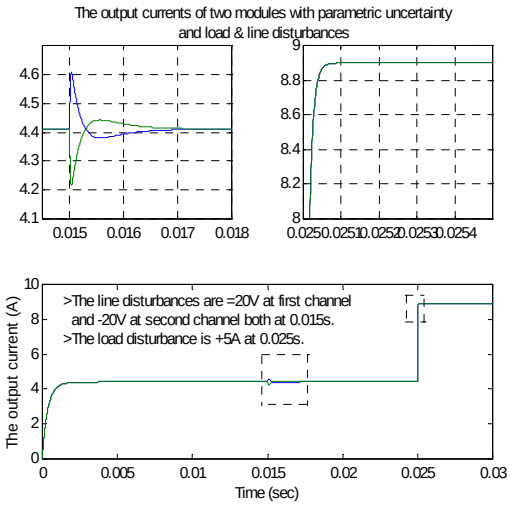

Fig. 12. The steady state and transient behavior of the output currents in the presence of line & load disturbances with uncertainty.