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3D SIMULATOR OF TRACK SYSTEMS IN SEMICONDUCTOR FABRICATION

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Abstract: This paper presents a 3D simulation environment for track systems in semiconductor fabrication. The track systems together with exposure tools carry out important functions of the photolithography process of semiconductor fabrication. The developed 3D track simulator can be used for design and evaluation of track systems, and their performance analysis. The main goal of the 3D track simulator is to provide a user with more accurate simulation environment for track systems. The developed 3D simulator consists of GUI (Graphic User Interface), scheduler, animator, and performance analyzer, where the animator part is constructed based on a discrete event simulation software, AutoMod, of Autosimulations. *Copyright © 2002 IFAC*

Keywords: Simulator, semiconductor manufacturing, virtual reality.

I. INTRODUCTION

A track system performs photolithography process with an exposure tool called stepper. Track system is a clustered equipment composed of indexer, process modules, buffers, and transfer robots. Fig. 1 shows the typical layout of a track system. We present a 3D simulation environment for the track systems in semiconductor fabrication. The track simulator can be used for design and evaluation of track systems, and their performance analysis.

The track system has complex process flows of wafers, which can be frequently changed depending on various wafer types. Scheduling of the track systems can be divided into two parts, that is, input release and dispatching. The former is to determine the type of a wafer and the time to be released into the track system. The latter is to select a wafer and an available process module for the next operation. Wein (1998) reports that good selection of scheduling rules in semiconductor fabrication may lead to 10-20% reductions in mean cycle time, and it is significantly beneficial to production smoothness and equipment utilization. A lot of scheduling rules are studied in the field of semiconductor industry

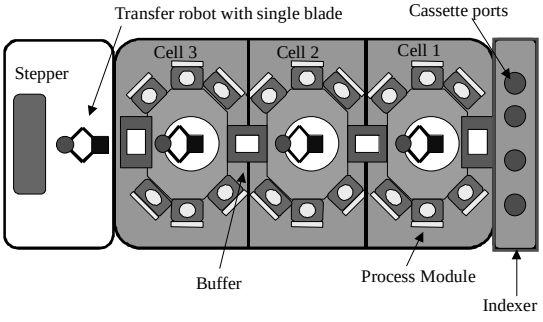


Fig. 1. Typical layout of a track system.

(Dabbas *et al.*, 2001; Hsih *et al.*, 1999; Thompson, 1996; Wein, 1988). However, it is difficult to select the scheduling rules appropriate for a given configuration of the track system.

Performance analysis is a useful function of the 3D track simulator, which provides important measures such as makespan, utilization of process modules, mean and standard deviation of flow time, etc. The developed simulator also provides graphically and statistically accurate simulation environment for track systems.

The track system is also called as a coater and developer where photoresist material is applied on a

wafer and then it is developed. Early track systems used sequential transfer technique, such as O-ring belt, air bearings, and walking beam systems, to move wafers from module to module. Random-access robotic system is recently employed to offer greater process flexibility (Biche, 1995).

Fig. 2 shows one of the widely used track system layouts in the current semiconductor fabrication. There are 4 cells, each of which is composed of a transfer robot, and several process modules or stepper. Process modules are composed of cool plates (CP), hot plates (HP or HHP), post exposure bake hot plates (PEB), edge exposures (EE), spin coaters (SC), spin developer (SD), and low-pressure adhesions (LPAH). These process modules are plugged into each cell with two floors, and the maximum number of configurable process modules is 16 for each cell. There are cassette indexers at one end of the track system and the opposite end is linked to an exposure tool. The three robots transfer wafers from module to module in each cell, or from cell to cell, and one robot moves wafers from track system to exposure tool and vice versa. There is a three-pin stage (IF) between cells and each stage can store one wafer at a time. A stacker (STK), 2 columns with 16 rows of three-pin stages, is located between the track system and the exposure tool to store wafers.

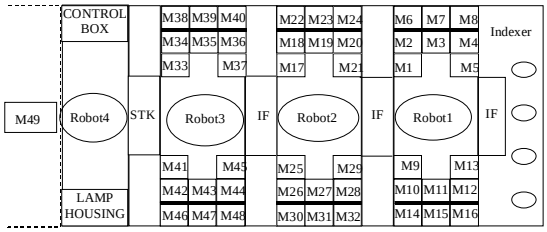


Fig. 2. A detailed layout of a track system.

II. 3D TRACK SIMULATOR

The developed 3D track simulator consists of four modules, i.e., Graphic User Interface (GUI), scheduler, animator, and performance analyzer. Fig. 3 depicts the architecture of the developed 3D track simulator. Users can enter information such as job type, lot size, layout and process routes through the GUI module constructed using Microsoft Visual Basic. The input data are conveyed to the scheduler and the animator. The animator uses software, AutoMod. The data transfer between GUI and AutoMod is implemented using ActiveX. The animator performs 3D simulation based on the on-line schedule generated by the scheduler. Users can evaluate various performance measures using the performance analyzer during or after the simulation.

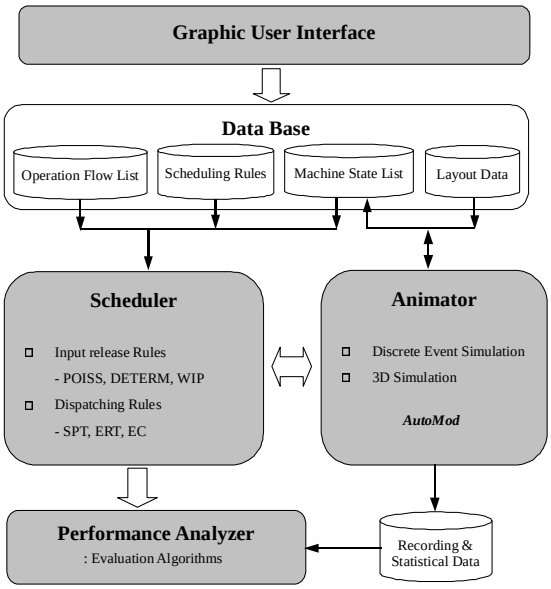


Fig. 3. The architecture of the 3D track simulator.

2.1 The Graphic User Interface (*GUI*)

The GUI module allows users to set up simulation conditions and parameters; scheduling rules, process routes of each wafer, processing time, and various machine parameters such as MTBF (Mean Time Between Failure) and MTTR (Mean Time To Repair). Fig. 4 shows the GUI module to set up the layout of the track system and to enter the operation data.

The main menu panel is to select the scheduling rules, i.e., input release rule and dispatching rule, and their parameters such as the number of WIP (Work-In-Process) and input interval time. Users can switch among the view options. The layout design panel is to configure locations of each process module in the track system. Finally, in the operation data input panel, users can enter detailed information of process flows of each wafer type, that is, the number of the total operations, the process modules required and their processing times for each operation step, MTBF, MTTF, etc. These operation data can be saved as an ASCII file, and used for the next simulation.

2.2 The Scheduler

The scheduler generates on-line schedules using the scheduling rules determined in the GUI module. There are two primary types of scheduling decisions, i.e., input release rule and dispatching rule.

Three input release rules, i.e., Poisson (POISS), Deterministic (DETERM), and WIP rules, are implemented in the developed 3D track simulator. The POISS rule releases wafers into the track system according to a Poisson distribution, and the DETERM releases wafers at fixed intervals. The WIP limits the total number of wafers currently in the track system, that is, a new wafer is released whenever a wafer finishes its entire operations and leaves the track system. For instance, WIP(k) implies that a new wafer should be released when the number of wafers in the track system drops to K-1. Wafers are released into the track system using DETERM until the current level of WIP in the track system is less than WIP(k).

The 3D track simulator includes three dispatching rules, i.e., SPT, EC, and ERT. The SPT selects the

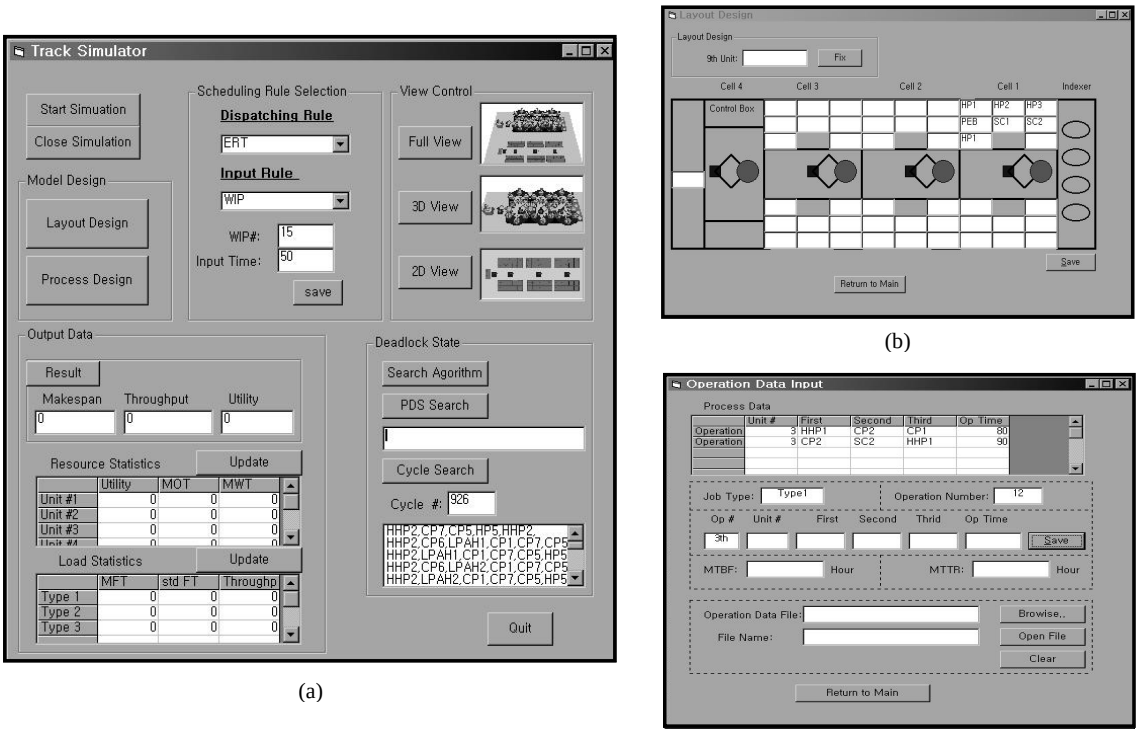


Fig. 4. GUI module. (a) Main menu. (b) Layout design. (c) Operation data input.

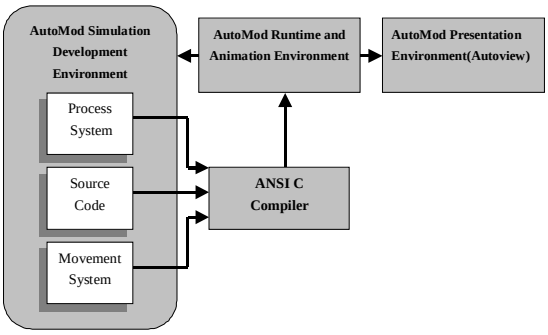


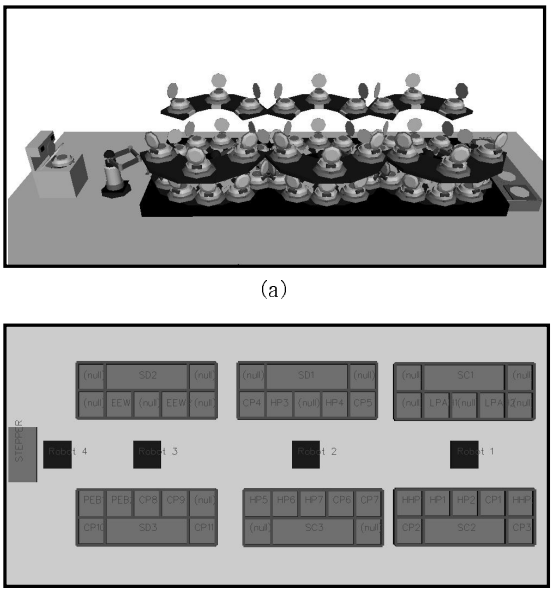
Fig. 5. Modular interaction of AutoMod.

wafer with the shortest processing time, and the EC selects the wafer with the earliest completed prior operation. Finally, ERT selects the wafer with the earliest releasing time into the track system.

2.3 The Animator

The animator presents a 3D graphic view of the simulation. AutoMod of Autosimulations, a 3D discrete event system simulation software is used for the animation (Rohrer, 2000).

The AutoMod model consists of three components, i.e., process systems, movement systems, and logic source code. The process system deals with general features required for graphic model of the track system, such as process modules and wafers. The movement systems are used for the transfer robots. Finally, the logic source code includes the scheduling logic that controls the flow of wafers.



(a)

(b)

Fig. 6. The graphic model of the track system. (a) 3D view and (b) 2D view.

All of the created components of the track system model are compiled into a simulation code using ANSI C compiler, and then it is passed to the runtime/animation environment. The runtime environment performs the simulation and animation concurrently. Fig. 5 depicts the general interactions among the AutoMod system components. Fig. 6 illustrates the constructed graphic model of the track system, using the AutoMod in 3D view and 2D view.

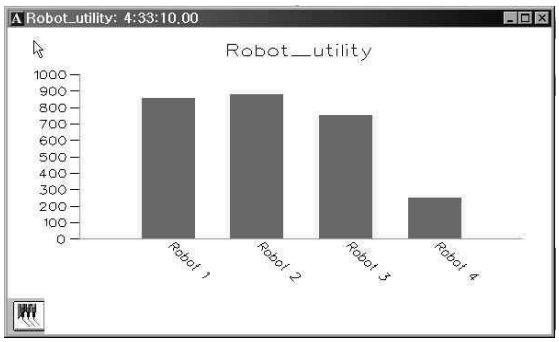


Fig. 7. Utilization graph of each transfer robot.

Table 1 Process flows of three wafer types

Op	TARC #1	TARC #2	BARC
Op 1	HHP1/HHP2 (80)	HHP1/HHP2 (80)	HHP1/HHP2 (80)
Op 2	LPAH1/LPAH2 (90)	LPAH1/LPAH2 (90)	LPAH1/LPAH2 (90)
Op 3	CP2/CP3 (60)	CP2/CP3 (60)	CP2/CP3 (60)
Op 4	SC1/SC2 (65)	SC1/SC2 (65)	SC3 (50)
Op 5	SC3 (50)	HP1/HP2 (90)	HP1/HP5 90()
Op 6	HP5/HP6 (90)	CP6/CP7 (60)	CP1/CP6 (60)
Op 7	CP10/CP11 (60)	SC3 (50)	SC1/SC2 (65)
Op 8	STEPPER (100)	STEPPER (100)	HP6/HP7 (90)
Op 9	PEB1/PEB2 (90)	PEB1/PEB2 (90)	CP10/CP11 (60)
Op 10	CP8/CP9 (60)	CP8/CP9 (60)	STEPPER (100)
Op 11	EEW1/EEW2 (90)	EEW1/EEW2 (90)	PEB1/PEB2 (90)
Op 12	SD1/SD2/SD3 (130)	SD1/SD2/SD3 (130)	CP8/CP9 (60)
Op 13	HP3/HP4 (90)	HP3/HP4 (90)	EEW1/EEW2 (90)
Op 14	CP4/CP5 (60)	CP4/CP5 (60)	SD1/SD2/SD3 (130)
Op 15			HP3/HP4 (90)
Op 16			CP4/CP5 (60)

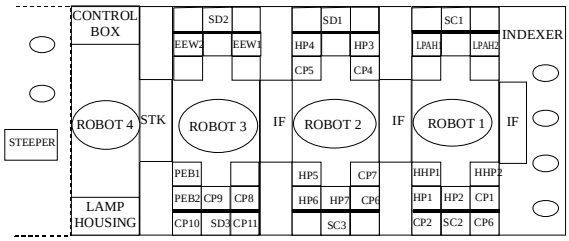


Fig. 8. Layout of the track system.

2.4 The Performance Analyzer

The developed simulator evaluates various performance measures used in the field of semiconductor manufacturing (Dabbas, 2001; Nehme *et al.*, 1994). The simulator records important time and state history data in the data base system during simulation.

The main performance measures of the track system include makespan, mean and standard deviation of flow time, throughput rate, utilization of the track system and each process module, bottleneck information, etc. The makespan is the completion time of the last wafer to leave the track system, and the flow time is the interval time between the release and completion of each wafer. The throughput rate is the number of produced wafers per unit time. For example, Fig. 7 shows the performance graph related to the utilization of transfer robots.

Table 2 Simulation result of single process: TARC#1

Input Rule	Dispatching Rule	Flow Time (seconds) Mean (Std. Devn.)	Utility	Throughput Rate (Wafers/hrs)
WIP	SPT	1560.1 (181.6)	0.3366	28.85
	EC	1944.7 (328.2)	0.3364	28.85
	ERT	1559.2 (182.0)	0.3366	28.85
DETERM	SPT	1713.0 (447.7)	0.3366	28.62
	EC	1951.9 (344.2)	0.3364	28.62
	ERT	1679.1 (428.8)	0.3364	28.62
POISS	SPT	2498.5 (637.1)	0.3330	28.54
	EC	2813.8 (1408.4)	0.2821	28.54
	ERT	2498.5 (632.7)	0.3330	28.54

Table 3 Simulation result of mixed process with WIP(20)

Dispatching Rule	Wafer Type	Flow Time (seconds) Mean (Std. Devn.)	Utility	Throughput Rate (Wafers/hrs)
SPT	TARC#1	1680.4 (258.9)	0.2939	28.47
	TARC#2	2007.0 (1292.4)		
	BARC	3150.2 (2730.5)		
EC	TARC#1	2363.4 (473.0)	0.2814	27.46
	TARC#2	2444.2 (365.6)		
	BARC	2612.3 (344.3)		
ERT	TARC#1	2508.3 (408.0)	0.2930	28.38
	TARC#2	1822.2 (326.2)		
	BARC	3226.1 (1306.9)		

III. EXPERIMENTS

This section presents simulation results using the track system reported in Yoon *et al.* (2000). There are three types of wafers for processing: TARC#1, TARC#2, and BARC. Table 1 shows the process flows of the three wafer types. TARC#1 and TARC#2 have 14 sequential operations, and BARC has 16 sequential operations. Each number in the parenthesis denotes the processing time of the corresponding operation in seconds. The wafers are packed in a cassette when they enter the indexer of the track system. Each cassette contains 25 wafers, that is, 10 TARC#1, 10 TARC#2, and 5 BARC. Fig. 8 shows the layout of the track system with 31 process modules and 4 transfer robots.

The simulation result for single process of TARC#1 is shown in Table 2. Three different dispatching rules are evaluated for each input release rule. The simulation result reveals that all the dispatching rules perform better with WIP input rule than with the other input release rules, for the flow time, utility, and throughput rate. The dispatching rule influences the mean and the standard deviation of the flow time. If the standard deviation of the flow time is small, supervisor can easily predict when a wafer will finish its operation.

Table 3 shows the result of the simulation with mixed wafer types. This simulation is performed with the input release rule WIP(20). The simulation result shows that EC rule gives the best standard deviation of flow time. Fig. 9 shows the comparison of the mean and the standard deviation of the flow time under each dispatching rule. The result of the simulation with mixed wafer types

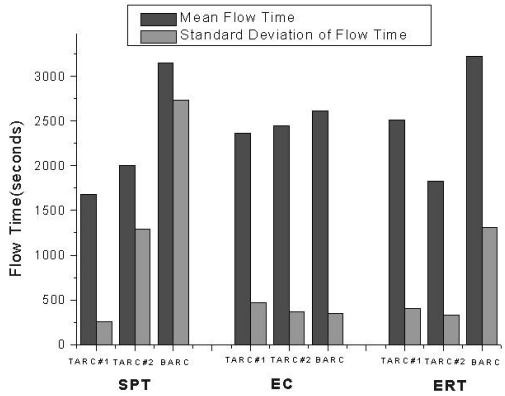


Fig. 9. Mean and standard deviation of flow time for mixed wafer types.

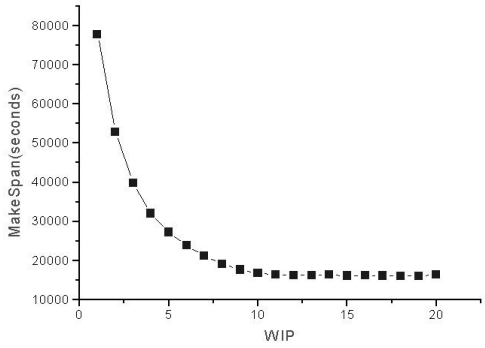


Fig. 10. WIP versus makespan in mixed wafer types.

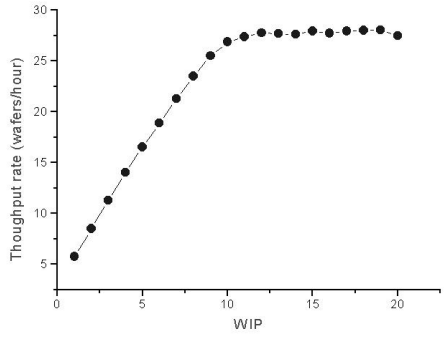


Fig. 11. WIP versus throughput rate in mixed wafer types.

shows that there are two overwhelming bottlenecks. That is, utilization of spin coater (SC3) and stepper is very high with 0.8174 and 0.7139, respectively. Since the stepper should keep high utilization rate considering its high cost, it is desired to put another spin coater in the track system to reduce the utilization of SC3. On the other hand, the simulation result shows that the utilization of spin developer (SD3) is close to zero. Therefore, it is recommended to replace the SD3 with another spin coater to balance between the utilization of spin coater and spin developer.

Fig. 10 and 11 show relationship of WIP versus makespan and throughput rate, respectively. They are plotted using the data obtained from simulation results of the mixed wafer types. The graphs show that the makespan and the throughput rate converge if the level of WIP becomes larger than 11. Thus, it is recommended to use WIP(11) for the input release rule.

IV. CONCLUSION

A 3D simulator of the track systems is developed. The developed simulator is focused on a specific equipment, track system, rather than general manufacturing systems to provide graphically and statistically more accurate model. Users can directly use the developed simulator with the 3D graphic models similar to the real systems, to evaluate scheduling rules and analyze various performance measures. The experiments using the example track system shows that the developed simulator is effective in comparing the effects of scheduling rules and analyzing various performance measures such as throughput rate, flow time, utilization, etc. The developed track simulator can be also used for manufacturing education and training due to its simple easy-to-use operation interface.

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