DIGITAL REPETITIVE CONTROL OF A SINGLE-PHASE CURRENT ACTIVE FILTER

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Abstract

Shunt active power filters are proved as useful elements to correct the distorted currents caused by nonlinear loads in power distribution systems. This work presents an all digital approach, based on the repetitive control technique, for their control. The design is performed for the particular case of single-phase shunt active filter with a full-bridge boost topology. Several simulation results are also presented to show the good behavior of the closed loop system.

1 Introduction

In the last years, typical power distribution systems have a proliferation of nonlinear loads such as power electronic converters. This fact has deteriorated the power quality of electrical power systems. In particular, voltage harmonics and power distribution equipment problems result from the current harmonics produced by nonlinear loads. This fact has lead to the proposal of more stringent requirements regarding power quality like the collected in the standards IEC-61000-3-{2,4} and IEEE-519.

A lot of work have been done in the area of active filter control and among others could be cited [1, 2]. But it seems that, as a conclusion, the most important fact is the necessity of high gain current control loops [2]. Perhaps the easiest way to obtain it is using some kind of hysteresis controller (or relay controller). However, in the digital control area, there is a technique called repetitive control that allows to design control loops with high gain in the harmonic frequencies of a fundamental one. This approach can supply the necessary high gain requirements of the current control loops in active filters. Previously, this technique has been applied to inverter and PWM rectifier control [8, 7]. This work uses the repetitive control technique to design a high gain current digital control loop for a single-phase shunt active filter.

This paper is organized as follows. Section II presents the problem and the specifications for the closed loop system. Section III shows the multi-loop controller design. Section IV collects several simulation results of the system. And, finally, Section V summarize the results of this work.

2 Problem statement and specifications

Fig. 1 shows the layout of the system under study: a mixed linear and nonlinear load connected to a power source with an internal impedance. The nonlinear load draws a distorted current waveform (non-sinusoidal shape) with the same fundamental period as voltage but with high order harmonic content. Also, the linear load can demand some reactive power from the source and, in consequence, its sinusoidal current has a lag with respect to the voltage waveform.

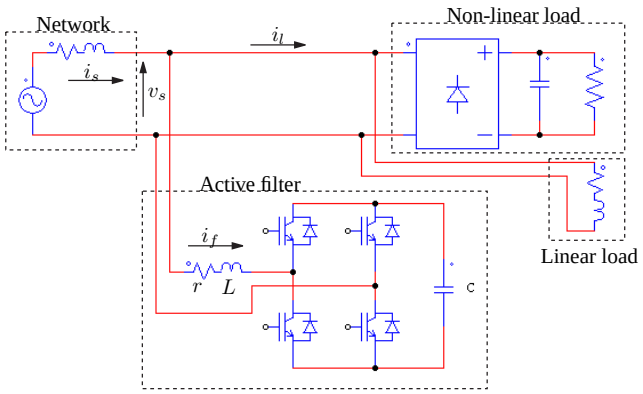

Figure 1: Single-phase parallel active filter connected to a network with a linear and a non-linear load.

The averaged (at the switching frequency) model of the full-bridge boost active filter is given by

$$L\dot{x}_1 = -rx_1 - x_2u + v_s \quad (1)$$
$$C\dot{x}_2 = x_1u \quad (2)$$

where x_1 is the inductor current and x_2 is the DC capacitor voltage; $v_s = E\sin(\omega_r t)$ is the voltage at network terminals; r sums the parasitic resistance of all the converter elements; and L and C stands for the inductor and the capacitor of the converter. The control variable u takes its value in the closed real interval $[-1, 1]$ and represents the averaged value of the PWM (pulse-width modulated) control signal injected to the real system.

The control objectives are: constant average value of the voltage at the DC bus capacitor, i.e. $< x_2 >_0^* = V_d$, and sinusoidal source current in phase with the voltage waveform, i.e. $i_s^* = I_d^*\sin(\omega_r t)$. These two objectives define a non-standard control problem: the first one is a regulation objective but the

second one is not a tracking specification because only a shape and not a function is desired, i.e. I_d^* is not known a priori and it must take the adequate value to maintain the power balance of the system. This special form for the problem specifications implies the particular structure of the controller loops described in the next section. It is important to remark that the controller structure will permit to overcome the inherent limits to the non-minimum phase characteristic of the boost full-bridge active filter.

3 Control Design

Assuming that $v = ux_2$ and $\mathbf{y} = [x_1, \frac{1}{2}x_2^2]'$ equations (1)-(2) can be restated as

$$L\dot{y}_1 = -ry_1 - v + v_s \tag{3}$$
$$C\dot{y}_2 = y_1 v \tag{4}$$

where y_1, y_2 are the inductor current and the DC bus capacitor voltage squared and divided by 2. The new input variable for the plant is v.

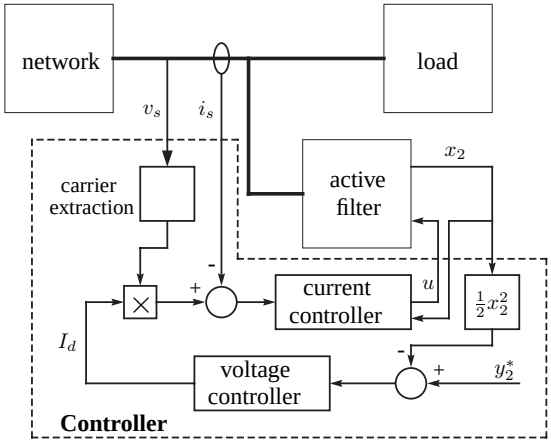

Figure 2: Controller block diagram showing the current and voltage loops.

The controller is composed by two digital control loops as it can be seen in Fig. 2. The inner loop is the current control loop. Its function is to shape the source current i_s to a sinusoidal in phase with the voltage source v_s. To get this objective a current sensor is placed on the network terminals and this current is used as the feedback signal in the current control loop. A point worthy of mention is that no current sensors are necessary at the load terminals nor at the active filter inductor. In this case, the load current is seen as a disturbance signal for the source current control loop, see Fig. 3. However, this approach has as drawback that the active filter and control loops dynamics affect the active power flow from the source to the load and then, the outer voltage loop must be slightly faster in order to cope this problem.The current control loop works at a sampling frequency equal to the switching frequency of the active filter.

The outer control loop is the voltage loop. Its main function is to maintain the DC bus voltage close to the reference value in spite of the load changes in the system. Since the inner current

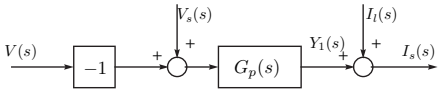

Figure 3: Block diagram for equation 3.

loop controls the source current and its reference is the output of the voltage controller multiplied by a sinusoidal carrier signal in phase with the source voltage, to keep the DC bus voltage close to the reference value can be seen as a way to assure the power balance of the active filter plus load set.

3.1 Current loop design. A repetitive control approach

The continuous time transfer function that describes the unperturbed dynamic behavior of equation (3) is

$$G_p(s) = \frac{Y_1(s)}{V(s)} = \frac{-1/r}{\frac{L}{r}s + 1}. \tag{5}$$

This transfer function is sampled with a zero-order hold at a sampling frequency equal to the switching frequency of the converter giving as a result $G_p(z)$, and then this function is taken as a plant for the digital current controller design as it can be seen in Fig. 4.

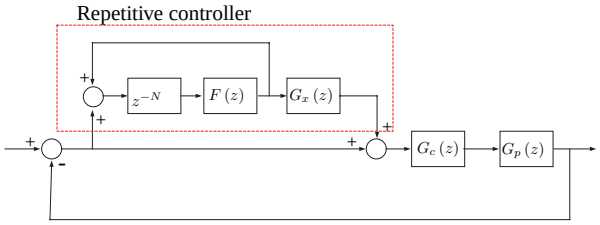

Figure 4: Repetitive controller scheme for the current loop.

Repetitive controllers are usually implemented in a "plug-in" fashion, that is to say the repetitive compensator is used to augment an existing nominal controller, $G_c(z)$ (Fig. 4). This nominal compensator is designed to stabilize the plant, $G_p(z)$, and provides disturbance attenuation across a broad frequency spectrum. This scheme was first introduced by Inoue et al. [5].

The repetitive controller is composed by the combination of three lineal systems: a time delay z^{-N} which, together with the positive feedback loop, is in charge of introducing infinite gain at harmonic frequencies; a null-phase FIR low pass filter $F(z)$ which reduces the gain of the abovementioned loop at those frequencies where system behavior is not properly modelled and; finally, a linear system $G_x(z)$ which is designed to assure closed loop stability. It is important to remark that the FIR filter $F(z)$ reduces the repetitive loop gain to finite values for all the frequencies endowing it with a general low-pass shape. In order to obtain a stable closed-loop system the sufficient conditions of Proposition 1 can be used.

Proposition 1 ([3]) *The closed-loop system of Fig. 4 is stable if the following conditions are fulfilled:*

1. *The closed loop system without the repetitive controller is*

stable, i.e. $G_o(z) \triangleq \frac{G_c(z)G_p(z)}{1+G_c(z)G_p(z)}$ *is stable.*

2. $\| F(z) \|_\infty < 1$.
3. $\| 1 - G_o(z) G_x(z) \|_\infty < 1$, *where* G_o *is the closed loop transfer function without the repetitive plug-in controller and* G_x *is a design filter to be chosen.*

Comments: (with respect to the conditions stated in previous Proposition)

- *Cond. 1*: This can assured by designing $G_c(z)$ properly. It is advisable to design the controller $G_c(z)$ with a higher enough robustness margin.
- *Cond. 2*: There is no problem about the causality of $F(z)$ because it is series connected with the delay z^{-N} and the repetitive loop will be executed as a whole in controller real-time operation.
- *Cond. 3*: One trivial structure which is often used is [6]: $G_x(z) = k_r G_o(z)^{-1}$. This structure can only be used if G_o is a minimum-phase transfer function. Otherwise, other techniques should be applied in order to avoid closed-RHS plane zero-pole cancellations [6]. Also, there is no problem with the no causality of $G_x(z)$ by the reason exposed in aforementioned comment.
- As in [4], k_r must be designed looking for a trade-off between robustness and transient response.

In this work the plant $G_p(z)$ has no zeros and the designed controller $G_c(z)$ is a minimum-phase first order lag controller, specifically $G_c(z) = -\frac{0.0135z-0.01}{z-0.905}$. Then, the closed-loop function $G_o(z)$ is a minimum-phase function and there is no problem choosing $G_x(z) = k_r G_o(z)^{-1}$. The assigned value for k_r is 0.2 and the null phase FIR low pass filter selected is $F(z) = \frac{1}{4}z + \frac{1}{2} + \frac{1}{4}z^{-1}$.

3.2 Zero Dynamics

In this section the zero dynamics is analyzed; steady-state controls $I_d = I_d^*$ and $u = u(t)$ such that the specifications hold are assumed. Then, the dynamics of x_2 is proved to be periodic and the value of I_d^* is obtained as well.

Proposition 2 *Let* $x_1 = i_s^* - i_l = I_d^* \sin(\omega_r t) - i_l(t)$ *where* $i_l(t)$ *is a periodic signal with period* $T = \frac{2\pi}{\omega_r}$, *then*

$$\left.\frac{C\,x_2^2}{2}\right|_{t_0}^{t_0+T} = \int_{t_0}^{t_0+T} E\,\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt - \int_{t_0}^{t_0+T} r\,(I_d^*\sin(\omega_r t) - i_l(t))^2 dt$$

Proposition 3 *The following statements are equivalent*

- $x_2(t)$ *is* T*-periodic.*
- $\int_{t_0}^{t_0+T} E\,\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt - \int_{t_0}^{t_0+T} r\,(I_d^*\sin(\omega_r t) - i_l(t))^2 dt = 0.$
- $x_2((k+1)T) = x_2(kT)$.

As conclusion, let be assumed control inputs u and I_d such that x_1 converges to $I_d^*\sin(\omega_r t) - i_l(t)$ and $\langle x_2 \rangle_0 = x_2^*$. Then I_d converges to I_d^* which in turn satisfies

$$\int_{t_0}^{t_0+T} E\,\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt - \int_{t_0}^{t_0+T} r\,(I_d^*\sin(\omega_r t) - i_l(t))^2 dt = 0,$$

and x_2 converges to a periodic function of the same fundamental frequency as x_1.

3.3 Voltage loop design

Let us take for simplicity $r = 0$. Then, the output voltage dynamics can be sampled with sampling period T, which yields the digital dynamics

$$C(z-1)Y_2(z) = \frac{ET}{2}\left(I_d(z) - b\right)$$

where $I_d(z)$ is the z-transform of the modulating signal in the AM-modulator (Fig. 2) and b is the coefficient of $sin(2\pi t/T)$ in the Fourier series expansion of the load current. The losses in the inductor, represented by $r \neq 0$ can be considered as an additive disturbance in the digital system. Thus, a classical PI controller will regulate y_2 to the desired value y_2^*. Namely,

$$I_d(z) = k_p(Y_2^*(z) - Y_2(z)) + k_I\frac{z+1}{z-1}(Y_2^*(z) - Y_2(z))$$

4 Simulation results

The controller designed in the previous section has been tested in simulation with the specific values given in Section 3.1. It is important to remark that the simulated model has been coded so close to reality as possible. In this context, the simulation model includes the PWM modulator (switched model of the active filter) and the physical parameters of the system correspond to the experimental setup under construction. Also, the simulation model includes a tuned (LC) filter at network terminals to reduce the current ripple at the fundamental harmonic of the switching frequency.

The values of the parameters are: active filter ($r = 0.034\Omega$, $L = 1\text{mH}$, $C = 10000\mu\text{F}$); rectifier (non-linear load) ($C = 1500\mu\text{F}$, $R_{load} = 24\Omega$ (full-load)), also the rectifier has an inductor (0.2mH) in its AC side to limit the derivative of the rectifier current; source ($V_s = 220\text{VRMS}$, 0.3Ω network impedance) and switching frequency (20 KHz).

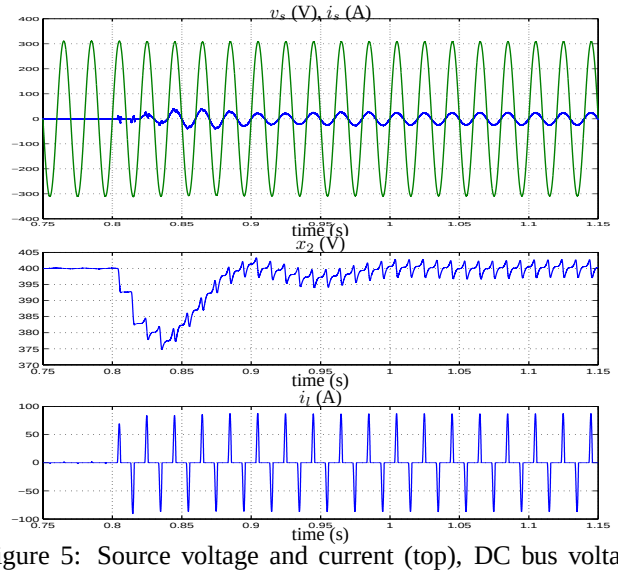

Figure 5: Source voltage and current (top), DC bus voltage (middle) and load current (bottom) when the non-linear load goes from no-load to full-load condition.

Fig. 5 shows the source voltage and current, the DC bus voltage and the load current when the rectifier goes from no-load to full-load condition. As it can be seen, the source current achieves the steady-state after six 50 Hz periods and the DC bus voltage overshoot is under 7% and 60 V up from the DC bus boost condition voltage. The maximum value of the time derivative of the load current is about 90 KA/s and the active filter is able to compensate it. Fig. 6 shows the source voltage and current, the DC bus voltage and the load current when the rectifier goes from full-load to no-load condition. The results are qualitatively very similar to the previous case showing that the designed controller performs well regardless of the direction of load changes. The THD value of the source current at full non-linear load is 1.9% and the power factor at network terminals is 0.99.

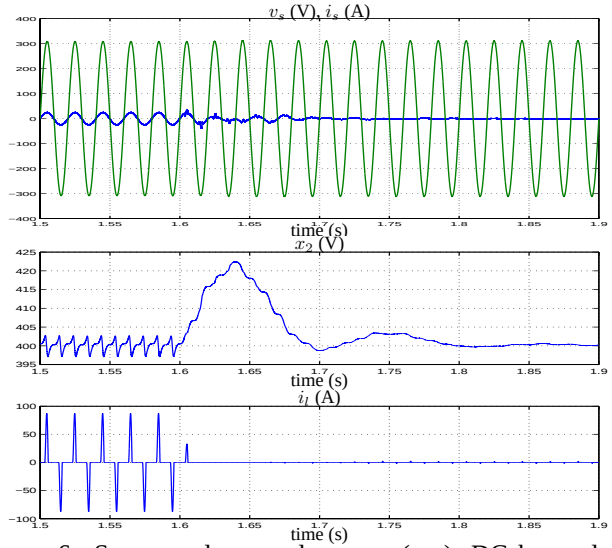

Figure 6: Source voltage and current (top), DC bus voltage (middle) and load current (bottom) when the non-linear load goes from full-load to no-load condition.

5 Conclusions

The paper shows the design of an all digital controller for a parallel active filter. The inner current control loop is designed using a digital repetitive control approach that, as the simulation results show, has a very good behavior shaping the source current. The high loop gain injected by the repetitive controller at the fundamental and harmonic frequencies of network frequency assures the good tracking of the reference current and the rejection of the high order harmonics of the load current. In the other hand, the external slow dynamics voltage loop assures the active power balance of the whole system adequately rejecting the load variations.

Acknowledgments

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