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A Sampled-Data Approach to DC-DC Buck Converter Design

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Abstract— **This paper examines the design of digital compensators for high frequency switching dc-dc buck converters. While a high sampling frequency is desirable for digital controllers to minimize intersample effects and recover the performance of the analog compensator (e.g. regulation, robustness with respect input voltage and load fluctuations), finite wordlength effects (i.e. binary approximation/truncation) become more pronounced when faster sampling rates are used. High sampling rates are also accompanied by larger power consumption. When low sampling rates are used, (appropriate truncation algorithms) permit the use of fewer bits to represent compensator coefficients. This reduces final chip area, power consumption, and cost - all very important for application-specific integrated circuit (ASIC) applications. This, however, comes at the expense of performance degradation because of zero-order-hold (ZOH) phase lag and intersample effects. This is a fundamental limitation associated with the traditional two-step design procedure - analog-design followed by conversion-to-digital. While one can compensate for the effects of the ZOH/intersample behavior, direct discrete-time design approach is more systematic. It must be noted, however, that even a direct discrete-time design approach has fundamental limitations. This is because such an approach does not directly take into account intersample behavior. Because of this, the direct design approach may result in unnecessarily (conservatively) high sampling rates. In view of this limitation, we propose the use of direct sampled-data design techniques which use "lifting" concepts that capture the periodic structure of the sampled data system in order to obtain a tractable optimization problem that accommodates meaningful (weighted $\mathcal{H}^\infty$) closed loop performance specifications as well as sample rate and intersample behavior. The design obtained is similar to the discretized classical designs complexity-wise - but operates at a much lower sampling rate. FPGA implementation data are presented for each design. Comparisons demonstrating the benefits of the sampled-data approach in achieving reasonable trade-offs are presented. Other issues addressed include: finite word length effects, controller complexity and realization.**

I. INTRODUCTION

Motivation. The demand for smaller, reliable, high speed, efficient, low cost pulse width modulator (PWM) dc-dc power converters that are very accurate and robust to anticipated uncertainties (e.g. input voltage fluctuations, load variations, parametric uncertainty, etc.) has increased steadily as they are used in the majority of dc-dc conversion applications. Feedback compensation is essential to meet performance specifications. Because of increasing performance requirements, the need for a compensator design methodology that systematically addresses the above issues is needed. This motivates the work reported in this paper.

DC-DC Converter Digital Compensation. This paper focusses on the design of digital compensators for a PWM dc-dc buck converter. Digital compensator implementations offer several advantages over traditional analog compensator implementations as reducing design cycle time,offer significantly more control functionality (e.g. ability to implement very sophisticated nonlinear control laws, monitoring, failure diagnosis, etc.), less sensitive to noise, easier to integrate with other digital subsystems.

It should be noted, however, that to date cost-performance issues have precluded wide-spread rapid transition to digital. This is primarily associated with the speed, resolution, complexity, cost, and power consumption issues. Digital implementations are also accompanied by finite word length, signal quantization, and arithmetic effects (e.g. fixed-point) that introduce nonlinear behavior (e.g. limit cycles) [1]. This too increases the up front modelling effort, the design effort, and the complexity of the final design - particularly when very demanding design specifications must be met.

Traditional Design Approaches. Traditionally, there have been two methods for designing such controllers. One is based on designing an analog controller and then discretizing [2]. The other is based on designing a direct discrete-time controller [3]. While both methods have proven to be valuable tools and, in principle, can address most aspects of the associated PWM "sampled-data" problem, they both suffer from a fundamental limitation.

Because these methods do not take into account intersample behavior , they can result in unnecessarily (conservatively) high sampling rates.

In PWM applications, this can result in excessive power consumption and unacceptable sensitivity to finite word length implementations (i.e. coefficients truncation) [4]. Lower sampling rates reduce power consumption, fewer bits to represent compensator coefficients reduces final chip area and cost - all very important for ASICs.

Direct Sampled-Data Design Approach. Given the above, we consider a direct sampled-data approach based on the novel analysis and design ideas presented within [5] [6]. The ideas exploit "lifting concepts" that directly accommodate intersample behavior. The main idea is that the time-varying periodic D/A-plant-A/D (sampled-data) system may be "lifted" to yield an LTI plant model upon which a design can be based[7]. The only drawbacks of this approach are

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that it requires a broader mathematical foundation to develop the ideas and possibly increased controller complexity to accommodate lower sampling rates. The methods described within [5] also permit one to address meaningful (weighted $\mathcal{H}^\infty$-like) closed loop performance specifications.

Contributions of Work. We focus on buck dc-dc converters [8] because they are simple, widely used, and they (more or less) capture the general difficulties associated with dc-dc converter design/compensation. All compensator designs which we examine are based on models obtained using classical averaging theory. The main contributions of this work are as follows:

- *Sampled-Data Design.* We show how modern sampled-data concepts may be used to obtain a digital compensator that addresses intersample behavior in order to meet meaningful closed loop (frequency domain) performance specifications while operating at reasonably low frequencies. A buck converter is used to illustrate the approach. The resulting design is compared to comparable bandwidth classical designs.
- *Experimental Data.* Linear and Nonlinear simulations, exploiting Xilinx' new System Generator tool, were performed which agree with the experimental data presented in the paper.

In short, the sampled-data approach is shown to be a powerful tool for systematically addressing important trade-offs that dc-dc converter designers must address.

Organization of Paper. Section II describes the buck converter to be examined. Controller designs are presented in Section III. Experimental FPGA implementation results are presented in Section IV. Finally, Section V summarizes the paper and presents directions for future research.

II. CONTROL SYSTEM STRUCTURE AND PLANT MODEL

A. Description of Buck Converter System

A typical buck converter circuit (with compensation) may be visualized as shown in Figure 1.

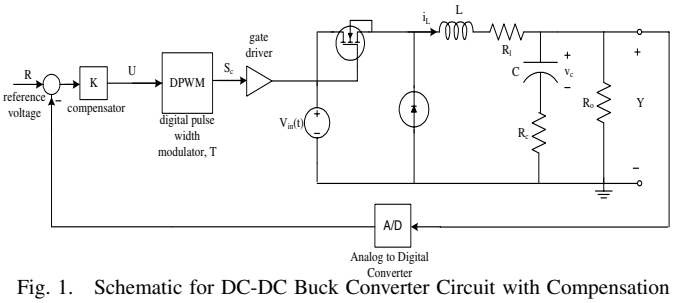

Fig. 1. Schematic for DC-DC Buck Converter Circuit with Compensation

B. Plant Model

We now present a small signal average LTI model for our plant - from the small signal control signal u_p to the small signal output voltage y_p. The model captures the effect of the MOSFET switch (a gain $V_{in_{DC}}$), the PWM (a gain $\frac{1}{V_m}$), and the LPF [8, pp. 336]. The plant model P will serve as the basis for compensator development. For the above parameters, P may be expressed in state space form as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(R_l + \frac{R_o R_c}{R_o+R_c}\right) & -\frac{1}{L}\left(\frac{R_o}{R_o+R_c}\right) \\ \frac{R_o}{(R_o+R_c)C} & -\frac{1}{(R_o+R_c)C} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (1)$$
$$+ \begin{bmatrix} \frac{V_{in_{DC}}}{V_m L} \\ 0 \end{bmatrix} (u_p + W_{d_i} d_i) + \begin{bmatrix} -\frac{R_o R_c}{(R_o+R_c)L} \\ \frac{R_o}{(R_o+R_c)C} \end{bmatrix} d_o$$

$$y_p = \begin{bmatrix} \frac{R_o R_c}{R_o+R_c} & \frac{R_o}{R_o+R_c} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \left[\frac{R_o R_c}{R_o+R_c}\right] d_o \quad (2)$$

where $x_1 = i_L$ is the inductor current, $x_2 = v_C$ is the capacitor voltage, d_i represents a fluctuation in the input voltage V_{in}, d_o represents a fluctuation in the load current, and $W_{d_i} = V_m \left[\frac{D_o}{V_{in_{DC}}}\right]$. d_i and d_o are viewed as disturbances. As such, they are nominally zero.

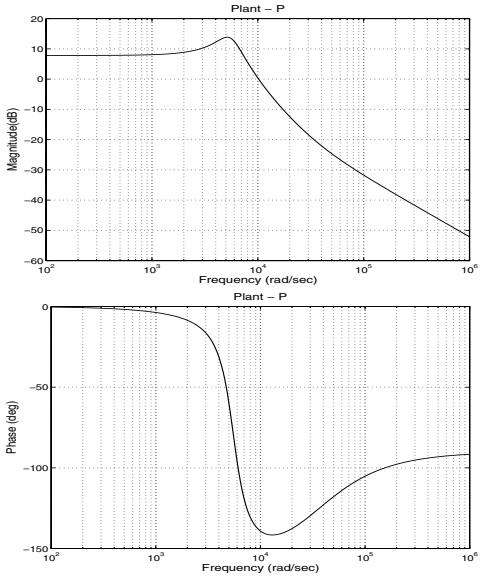

Fig. 2. Plant Frequency Response - P

Steady State Duty Cycle Analysis. The steady state duty cycle satisfies $Y_o = \left(\frac{R_o}{R_o+R_l}\right) V_{in_{DC}} D_o$ or:

$$D_o = \frac{Y_o}{\left(\frac{R_o}{R_o+R_l}\right) V_{in_{DC}}} = \frac{Y_o}{V_{in_{DC}}} \left(1 + \frac{R_l}{R_o}\right) \quad (3)$$

The following parameters will be used throughout the paper. The nominal input voltage $V_{in_{DC}} = 5V$, PWM peak sawtooth voltage $V_m = 2V$, desired output voltage $Y_o = V_o = 1.2V$, Inductance $L = 100\mu H$, Capacitance $C = 330\mu F$, parasitic series resistance for inductor $R_l = 0.16\Omega$, parasitic series resistance for capacitor $R_c = 0.1\Omega$, nominal output load Resistance $R_o = 10\Omega$. The frequency response [9] of the buck converter with the above parameters is shown in figure 2.

The LPF was designed using the ideas presented within [10]. Future work will closely examine optimal LPF design based on closed loop performance specifications and implementation constraints; e.g. inductor size.

C. DPWM and A/D Converter

Digital Pulse Width Modulator (DPWM) Resolution. Consider an N-bit DPWM. In such a case the duty cycle

D takes on 2^N possible discrete values and we say that the DPWM has a resolution of N bits. If f is the converter switching frequency, then one can implement an N bit DPWM using a clock with frequency $f_{clock} = 2^N f$; e.g. to achieve $f = 166.67$ kHz and $N = 8$ requires $f_{clock} = 42.667$ MHz. Similarly, if a clock frequency $f_{clock} = 30$ MHz is available and we implement a 166 kHz DPWM then the effective resolution is of the DPWM is

$$N = \log_2\left(\frac{f_{clock}}{f}\right) = \log_2\left(\frac{30}{0.16667}\right) = 7.49 \text{ bits.} \quad (4)$$

This is what we implemented within the lab. It should be noted that one can also exploit a tapped delay line to lower the required clock frequency [11].

A/D Converter Resolution. The resolution required by the A/D converter $n_{a/d}$ (i.e. number of output bits) is given by [12, 2001]:

$$n_{a/d} = int\left[\log_2\left(\frac{V_{max_{a/d}}}{H\Delta y_{max}}\right)\right] \quad (5)$$

$$= int\left[\log_2\left(\frac{V_{max_{a/d}}}{V_{ref}}\frac{Y_o}{\Delta y_{max}}\right)\right] \quad (6)$$

For our application, we have $V_{ref} = 1.2V$, $Y_o = 1.2V$, $\Delta y = 0.06V$, $V_{max_{a/d}} = 2V$. This yields

$$n_{a/d} = int\left[\log_2\left(\frac{2}{1.2}\frac{1.2}{0.06}\right)\right] = int[\,5.06\,] = 6\ bits. \quad (7)$$

We selected a 6 bit A/D converter that can operate at 166.67 kHz and 250 kHz.

III. CONROLLER DESIGNS

In this section the focus is on direct sampled data design. A 166kHz sampled data design is compared to several indirect sample data design (e.g. classical, $\mathcal{H}^\infty$) at 250 kHz. It should be emphasized that these indirect approaches do not yield an acceptable 166 kHz design unless additional work is done to accommodate ZOH and other phase lags associated with a digital implementation. In contrast, our direct approach addresses such lags directly. We wish to design discrete time controllers that achieve closed loop stability with continuous conduction mode(CCM) operation [8] (i.e. $i_L \geq 0$), good nominal output voltage regulation (ripple attenuation) - $y_{des} = Y_o \pm 12mV = 1.2V \pm 12mV$ (1%), good worst case output voltage regulation - $y_{des} = Y_o \pm 60mV = 1.2V \pm 60mV$ (5%), good attenuation of input voltage fluctuation disturbances -$V_{in} = 5 \pm 2V$ (40%), good attenuation of output load fluctuation disturbances - $i_{load} \in [0, 360]\ mA$ or $R_o \in [3.33, \infty)\Omega$, a reasonable tradeoff between sampling/switching periods and average power consumption p_c,robust with respect to dynamic uncertainty (e.g. controller computational delay, A/D phase lag, unmodelled parasitic L/C's, load impedance) -40° phase margin at gain crossover $f_g \approx 22KHz$), robust with respect to truncation of controller coefficients (12 significant bits), A/D signal measurement quantization (6 bits), and control signal (duty cycle) resolution (8 bits), frequency response robustness with respect to converter parametric uncertainty (i.e. R, L, C values, 5% tolerances).

In this paper, the digital control designs considered have a gain crossover frequency of 1.4×10^5 rad/sec (22.4 kHZ).

Induced $\mathcal{L}^2$ Sampled-Data. The design was obtained using the induced $\mathcal{L}^2$ ($\mathcal{H}^\infty$-like) sampled-data and lifting concepts within [5]. To precisely state how it was found, consider the sampled-data system in Figure 3.

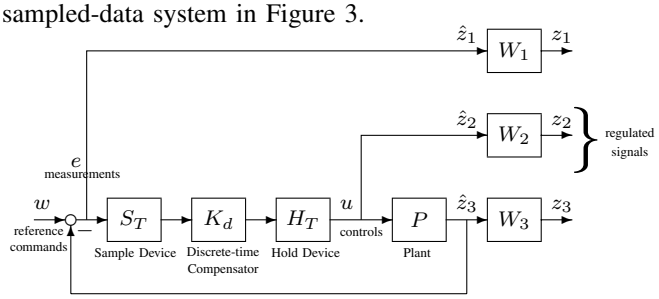

Fig. 3. Visualization of Weighted Mixed Sensitivity Sampled-Data Design

In this system (presented solely for design purposes), W_1, W_2, and W_3 are frequency dependent continuous-time weighting functions (i.e. s-domain transfer functions), S_T represents an ideal sampling device, H_T represents an ideal (zero order) hold device, T represents the sample time, K_d represents a linear shift invariant (LSI) discrete-time controller (to be designed).

Given the above, the design was obtained by solving the following weighted optimization problem:

$$\inf_{K_d}\{\gamma \mid \|T_{wz}\|_{\mathcal{H}^\infty} < \gamma\} = \inf_{K_d}\{\gamma \mid \left\|\begin{bmatrix} W_1 S \\ W_2 KS \\ W_3(1-S) \end{bmatrix}_T\right\|_{\mathcal{L}^2\to\mathcal{L}^2} < \gamma\}. \quad (8)$$

where $T_{we} = S \stackrel{\text{def}}{=} (I + PH_TK_dS_T)^{-1}$ denotes the sensitivity or reference to error operator, $T_{wu} = KS$ denotes the reference to control operator, $T_{w\hat{z}_3} = I - S$ denotes the complementary sensitivity or reference to output operator, $\mathcal{L}^2$ denotes the Banach space of Lebesgue square integrable (finite energy) functions [5], $\|G\|_{\mathcal{L}^2\to\mathcal{L}^2} \stackrel{\text{def}}{=} \sup_{x\in\mathcal{L}^2, x\neq 0} \frac{\|Gx\|_{\mathcal{L}^2}}{\|x\|_{\mathcal{L}^2}}$ denotes the induced $\mathcal{L}^2$ norm (or gain) of the operator G, and the optimization is carried out over all stabilizing LSI discrete-time controllers K_d. In short, the above problem seeks a compensator which minimizes the induced $\mathcal{L}^2$ gain of the transfer operator T_{wz} from w to z.

Comment 3.1: **(LTV Periodic Structure, LTI Version, Shaping Concepts)**

LTV Periodic Structure. It must be emphasized that the above sampled-data system is a linear time varying (LTV) system. This is because of the presence of S_T and H_T. However, because there is a base sampling frequency, the system is periodic. Given this, it can be "lifted" - through appropriate partitioning of inputs and outputs - to an LTI system.

LTI Version. When G is an LTI system, this norm given above is simply the $\mathcal{H}^\infty$ norm [13]; i.e. $\|G\|_{\mathcal{L}^2\to\mathcal{L}^2} = \|G\|_{\mathcal{H}^\infty} \stackrel{\text{def}}{=} \sup_\omega\ \sigma_{max}\ [\,G(j\omega)\,]$ where $\sigma_{max}\ (\,M\,) \stackrel{\text{def}}{=} \sqrt{M^HM}$ denotes the maximum singular value of the matrix M. For this reason, some refer to the resulting controller as an $\mathcal{H}^\infty$ sampled-data controller. Strictly speaking, this is not correct. A more appropriate term is induced-$\mathcal{L}^2$ sampled-data

controller. The LTI version of the above problem is addressed within [13].

Operator Shaping Concepts. The above framework permits a designer to "shape" the operators $T_{d_o y} = W_{d_o} S$, $T_{d_o u} = -KS$, $T_{d_i u} = -(1 - S)$ by appropriate selection of the weighting functions. Loosely speaking, one selects W_1 to be large over frequency ranges where $T_{d_o y}$ should be small. W_2 should be large over frequency ranges where $T_{d_o u}$ should be small. W_3 should be large over frequency ranges where $T_{d_i u}$ should be small. ∎

The design was obtained using $T = 6\mu sec$ (166.67 kHz) and the following weighting functions:

$$W_1 = \frac{1.05 \times 10^4}{s + 1.05 \times 10^4} \quad W_2 = 225\frac{10^9}{s + 10^9} \quad W_3 = [\ ]. \quad (9)$$

The design procedure may be described as follows.

1) Augment plant $P(s)$ with $\frac{10^6}{s}$ to obtain $P_o(s)$. This integral term, when absorbed into the final compensator will ensure perfect steady state voltage regulation, step input and output disturbance rejection, and good low frequency disturbance attenuation.
2) Form generalized plant, $G(s)$, with $W_i(s)$ and $P_o(s)$.
3) Transform $G(s)$ using bilinear transformation: $s = \frac{\hat{s}+p_1}{\frac{\hat{s}}{p_2}+1}$, $\hat{s} = \frac{s-p_1}{1-\frac{s}{p_2}}$ with $p_1 = -3250$, $p_2 = -1 \times 10^{25}$. For this selection of parameters, the above transformations become $s \approx \hat{s} - 3250$, $\hat{s} \approx s + 3250$. The transformation yields $\hat{G}(\hat{s})$.
4) Use $\hat{G}(\hat{s})$ to obtain a discrete-time controller $\hat{K}(\hat{z})$. This is accomplished by lifting the time varying periodic closed loop system to obtain an LTI system. After resolving (book-keeping/representation) issues [5], results from "standard" $\mathcal{H}^\infty$ theory may be applied to obtain $\hat{K}(\hat{z})$.
5) Convert $\hat{K}(\hat{z})$ to continuous time $\hat{K}_c(\hat{s})$.
6) Apply inverse bilinear transformation to $\hat{K}_c(\hat{s})$ to obtain $K_c(s)$.
7) Augment $K_c(s)$ with $\frac{10^6}{s}$ to obtain $K(s)$.
8) Discretize $K(s)$ to obtain $K_d(z)$.
9) Perform model reduction to obtain a lower order controller by removing the least significant controller poles.

The order of the $\mathcal{H}^\infty$ sample data controller is 6 (2^{nd} order plant, 1^{st} order integral augmentation, 1^{st} order weightings, (W_1 and W_2), 1^{st} order anti-aliasing filter). The 166 kHz design is the main design - meeting all design specifications while providing an acceptable tradeoff between power and implementation complexity (FPGA resources). At 166 kHz, the controller order was reduced to 3 to obtain

$$K_d(z) = 58.9241 \left[\frac{(z+1)(z-0.993)(z-0.3682)}{(z-1)(z+0.9999)(z-0.08277))} \right] \quad (T = 6\mu sec,\ f = 166.67kHz). \quad (10)$$

A. Frequency Responses

Frequency responses for each of the designs are now examined.

- **Open Loop.** Open loop magnitude and phase plots are given in Figure 4. Note that all three designs possess the same gain crossover frequency, namely $\omega_g \approx 1.41 \times 10^5$ rad/sec. The sampled-data design at 250 kHz is observed to have a much larger phase margin than the other three designs where the 166 kHz design has phase margin comparable to that of the other designs .

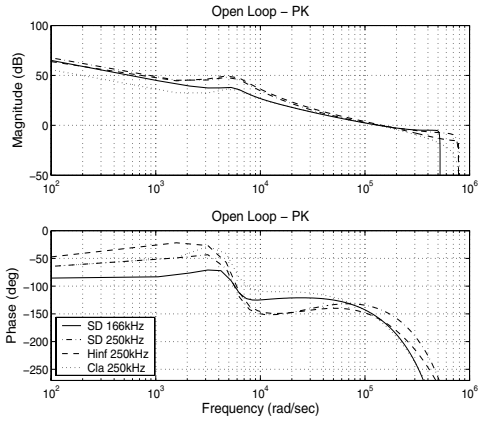

Fig. 4. Open Loop Frequency Responses - $L = PK$

- **Disturbance to Output.** Disturbance to output magnitudes for $T_{d_i y} = W_{d_i} PS$ and $T_{d_o y} = W_{d_o} S$ are given in Figure 5. The sampled-data design exhibits better disturbance attenuation. The sampled-data design is seen to exhibit worse performance (in comparison with the other designs) in the frequency range $\sim 10^4 - 10^5$ rad/sec. $T_{d_o y} = W_{d_o} S$ exhibits similar peaking to S (not shown).

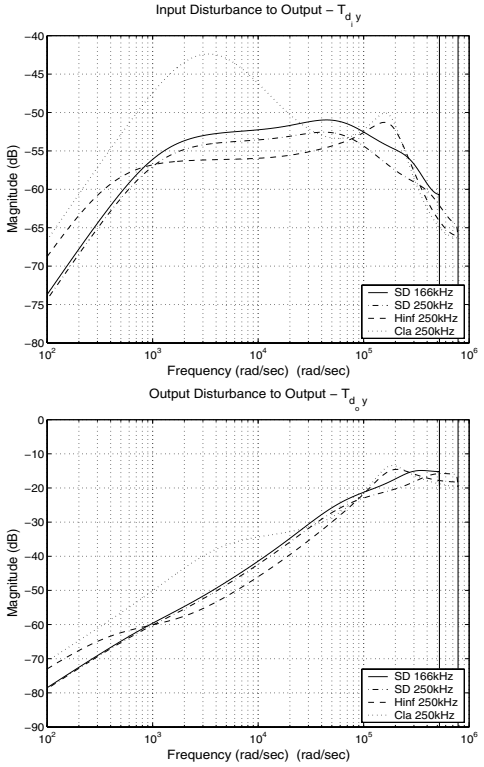

Fig. 5. Disturbance to Output Frequency Responses - $T_{d_i y}$, $T_{d_o y}$

From Figure 4, the phase margin of sample data 250 kHz $\mathcal{H}^\infty$ controller is larger than the other designs. Though the

phase margin of the Classical and $\mathcal{H}^\infty$ digital controllers at 250 kHz is comparable with that of the sample data $\mathcal{H}^\infty$ controller at 166 kHz, the performance of the digital controllers at 166 kHz is not comparable with that of 166 kHz Sample Data $\mathcal{H}^\infty$ controller for specified gain crossover frequency. This is because indirect approaches do not take inter sample behavior into account. In short, the (linear, small signal) frequency response properties of the sampled-data design are observed to be superior to those of the other two indirect designs.

IV. EXPERIMENTAL DATA FROM HARDWARE

This section presents data gathered from an FPGA implementations of our designs. All simulation results (e.g. linear and nonlinear) were validated within the laboratory.

The non-linear time responses were obtained using Xilinx' System Generator 6.1 - a Simulink-based (drag-and-drop) tool for high fidelity simulation of digital hardware implementations within field programmable gate arrays (FPGAs)[14]. Such simulations use the most detailed models and are therefore as close to the actual hardware as possible. More precisely, the following were captured within our hardware simulations: digital controller with finite wordlength coefficients (12 bits), 100 kHz DPWM using a 30 MHz clock (7.64 bits), ideal (lossless) switch, ideal (lossless) diode, LPF (including inductor and capacitive resistance), 6 bit A/D (2V range) and anti-aliasing filter. These non-linear simulations also show that the converter always operates in the continuous conduction mode even under worst case disturbances, the inductor current never reaching zero though we have diode in our circuit.

Summary of Experimental Data. Experimental data was gathered to assess nominal regulation and performance robustness with respect to input voltage and load current fluctuations. This was done for each of the digital designs discussed earlier. Figure 6 illustrates the output responses

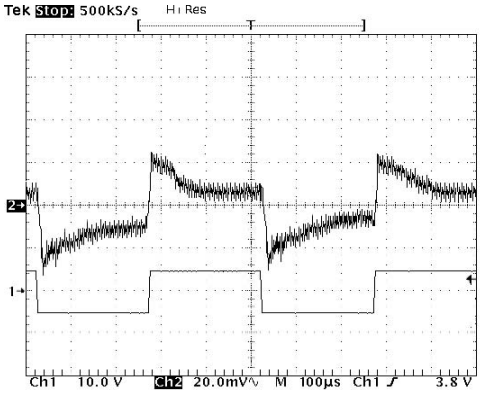

Fig. 6. Output Responses to Input Voltage Disturbance (5 ± 2V, 2kHz)

that result for a 5 ± 2V, 2 kHz, square wave input voltage disturbance. Figure 7 illustrates the output responses that result for a $R_o = 10\Omega$ to $R_o = 3.33\Omega$, 2 kHz, switching output load disturbance. For each design, the figures are consistent with linear and nonlinear (System Generator) simulations. The designs exhibited ripple on the order of ± 17 mV peak-to-peak and worst case peak-peak disturbance voltage of 55 mV as shown in figures 6 & 7.

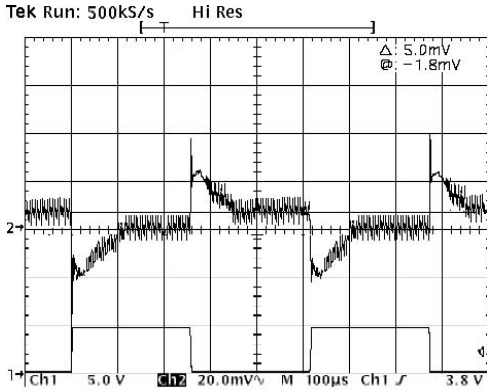

Fig. 7. O/p Responses to Load Disturbance ($R_o = 10\Omega = 3.33\Omega$, 2kHz)

Additional Observations. The following additional observations were made in the lab as well as through nonlinear System Generator simulations.

- *Finite Word Length Effects.* Each controller was implemented within the FPGA. We observed that 12 bit controller realizations based on "blind" truncation of associated difference equation coefficients resulted in very bad performance - including the loss of the integrator. This is expected, because such an approach destroys the pole-zero structure of the controller. Given this, each controller was implemented as a cascade of first order terms $\frac{z-z_k}{z-p_k}$ in order to preserve the pole-zero structure of the controller. By doing so, the sensitivity to coefficient truncation is significantly reduced. Twelve (12) bits were used to implement controller coefficients. The A/D supplies 6 bit binary numbers. The error signal (i.e. input to controllers) is a 7 bit number. 12 bits are also used to represent signals internal to the controllers. The output of the controller is truncated to 8 bits. This feeds our 7.49 bit DPWM. When 11 bit word lengths for compensator coefficients were used, the sampled data-designs were observed to be less sensitive than other designs. The performance degradation was significant though small than other designs: $\sim \pm 40$ mV worst case regulation for sampled-data design under a 5 ± 2 V 100 Hz input voltage square wave disturbance, $\sim \pm 45$ mV for other designs. For 10 bits, performance degradation was much worse - on the the order of 130 mV. Future work will examine optimal finite word length realizations and use of nonlinear methods (e.g. dither).
- *Controller Complexity.* An important metric in evaluating an FPGA-based digital controller implementation, is the amount of resources used on the FPGA board. Table I summarizes FPGA resource usage for each of the design implementations.
  The (second) slice column in Table I summarizes the total resources consumed on the FPGA by a given design. The sampled-data design at 150 kHz is a 5^{th} order design where as the other designs are of 3^{rd} order. The slice column shows that the 5^{th} order sampled-data design consumes about 6% more of the total

available resources than the other 3^{rd} order designs which is about 27% overhead for the 5^{th} order. This is not significant given today's ASIC manufacturing technologies. Each design uses 32 Input Output Blocks (IOB) of the total available 170.

TABLE I

Device Utilization in v300pq240-6 for Different Compensators.

Compensator (Available)	Slices (3072)	Flip Flops (6144)	4 Input LUT (6144)
$\mathcal{H}^\infty$ SD(150kHz)	973(32)	179(2)	1963(32)
$\mathcal{H}^\infty$ **SD(166kHz)**	773(26)	128(2)	1768(29)
$\mathcal{H}^\infty$ SD(200kHz)	768(25)	132(2)	1720(28)
$\mathcal{H}^\infty$ SD(225kHz)	753(25)	130(2)	1733(28)
$\mathcal{H}^\infty$ **SD(250kHz)**	767(25)	124(2)	1786(29)
$\mathcal{H}^\infty$ **(250kHz)**	758(25)	118(2)	1836(30)
Classical(250kHz)	788(26)	127(2)	1754(29)

In general, controller complexity for the sampled-data designs are expected to be non-decreasing functions of the sampling period. This is because lower sampling frequencies result in more ZOH-lag which, roughly speaking, must be compensated for via additional low frequency lead and high frequency roll-off (to achieve a strictly proper design). For our sampled-data design, complexity changed very little as we lowered the sampling frequency.

TABLE II

Power Consumption in v300pq240-6 for Different Compensators.

Compensator	d_i Power(mW)	d_o Power(mW)
$\mathcal{H}^\infty$ SD(150kHz)	25	23
$\mathcal{H}^\infty$ **SD(166kHz)**	24	23
$\mathcal{H}^\infty$ SD(200kHz)	27	25
$\mathcal{H}^\infty$ SD(225kHz)	29	26
$\mathcal{H}^\infty$ **SD(250kHz)**	31	29
$\mathcal{H}^\infty$ **(250kHz)**	31	29
Classical(250kHz)	31	29

- *Steady State Average Power Consumption.* Steady state average power consumption is another important metric in evaluating a design. The table II provides the average power consumption in the FPGA for different controllers due to input and output disturbances applied at 2kHz. Assuming a lossless switch and diode, the approximate steady state average power consumption (in $R_l = 0.16\Omega$, $R_c = 0.1\Omega$, and $R_o = 10\Omega$) for the three designs were as follows: $p_{R_l} = 2.304$ mW, $p_{R_c} = 1.21$ mW, $p_{R_o} = 144$ mW. Future work will address average power consumption for each design as well as incorporating switch and diode losses.
- *FPGA Power Vs Frequency Vs Area.* Fig 8 shows that as frequency is decreased, the power for the (d_i,d_o) scenarios considered decrease (as expected). The figure also shows the complexity increases as frequency is reduced. This too is expected.

V. SUMMARY AND FUTURE DIRECTIONS

This paper has considered the design of digital compensators for a dc-dc PWM converter. While focus is placed on a buck converter, the methods presented can be applied to other converter types. The main method presented is a direct sampled-data design methodology based on weighted $\mathcal{H}^\infty$ optimization that directly takes into account sampling frequency and intersample behavior by exploiting "lifting" concepts. Experimental results demonstrate how the methodology may be used to obtain a design with an acceptably low sampling frequency that yields acceptable intersample behavior and closed loop performance in the presence of input voltage and load fluctuations. Future work will examine methods for systematizing the selection of appropriate weighting functions to meet performance specifications for buck and other converter types.

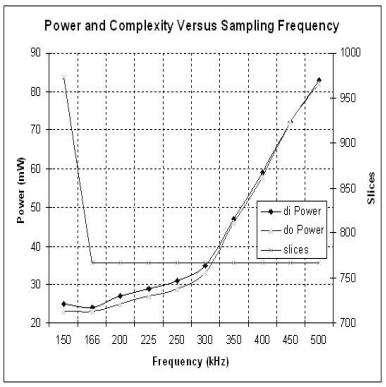

Fig. 8. Power and Complexity Versus Sampling Frequency in the FPGA

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