359a Integration of Metal-Catalyzed Semiconductor Nanowires [Invited]

Ted Kamins

Self-assembled, one-dimensional nanostructures are being considered as possible device elements to augment and supplant conventional electronics and to extend the use of CMOS beyond the physical and economic limits of conventional technology. Both carbon nanotubes and semiconductor nanowires are being extensively discussed. Facile integration of the one-dimensional nanostructures with conventional electronics will speed their acceptance and incorporation. In particular, easy connection between the nanostructures and conventional silicon integrated circuits will be important. This paper will focus on the challenges to be overcome to form integrated systems containing semiconductor nanowires, particularly Si nanowires, and will emphasize integration of nanowires at their growth location.

Nanowires have been grown by several different techniques, including laser ablation and chemical vapor deposition (CVD), with the latter being the most widely used technique. CVD is familiar throughout the semiconductor industry and allows control of the deposition process and nanowire composition. When the nanowire is grown on a crystalline substrate, the growing nanowire can continue the substrate crystal structure so that the nanowire grows "epitaxially" on the substrate in a direction determined by the nanowire preferred crystal growth orientation and the orientation of the corresponding directions in the substrate. Thus, nanowires can be grown perpendicular to a plane surface by choosing the surface orientation to correspond to the nanowire preferred growth direction.

When doped Si nanowires are grown vertically on a substrate of the same conductivity type, the grown connection between a nanowire and the substrate is ohmic, as is reasonable because of the intimate epitaxial connection formed between the nanowire and the substrate. When the nanowire is doped oppositely from the substrate, a rectifying junction is obtained. The dopant type can be changed part way through the growth of the nanowire, creating a p-n junction with a rectifying characteristic within the nanowire itself. The conductance of a vertical nanowire can be modulated by a horizontal gate electrode surrounding the nanowire. When nanowires are grown vertically from a horizontal surface, the second electrical contact is usually made after nanowire growth by depositing a metal on the exposed end of a nanowire. However, connections can be formed to both ends of a nanowire by growing it laterally from a vertical surface formed by etching the top Si layer of a silicon-on-insulator structure into isolated electrodes.

Because the ratio of surface to volume in a thin nanowire is high, conduction through the nanowire is very sensitive to surface conditions, making it effective as the channel of a field-effect transistor or as the transducing element of a gas or chemical sensor. As the nanowire diameter decreases, a greater fraction of the mobile charge can be modulated by a given external charge, increasing the sensitivity. To be effective, the charge must be physically close to the nanowire so that the majority of the compensating charge is induced in the nanowire, rather than in other nearby conductors, and so that ions in solution do not screen the charge by terminating the electric field lines before they enter the nanowire. Because only induced charge is being sensed, a coating that selectively binds the target species can be added to the nanowire surface to differentiate between different species in the fluid being measured.

Compound semiconductor nanowires can also be grown on Si substrates. The small diameter of a nanowire allows relief of the stress from even highly lattice-mismatched materials, permitting growth of high-quality, single-crystal nanowires of many compound semiconductors on Si. In addition to growing vertically on a horizontal surface, InP nanowires can also be grown laterally between two vertical Si surfaces separated by a gap and attach to the Si surface across the gap. However, the electrical connection between the Si and the compound semiconductor needs to be considered carefully. Both the expected bandgap offsets at the heterojunction and interface states may influence the behavior.

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