313b Fabrication and Evaluation of Silicon-on-Diamond Wafers

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Silicon on Diamond (SOD) is proposed as a superior alternative to conventional silicon and Silicon on Insulator (SOI) technology for silicon-based electronics. In this paper we present a novel SOD structure, in which the active Si layer is in direct contact with a thick, free-standing, highly oriented diamond (HOD) layer that is directly attached to a heat sink. Two different fabrication schemes are investigated: (1) direct growth, where Si-device layer makes contact with the nucleation side of the diamond layer and (2) wafer fusion, where Si device layer makes a direct contact with the diamond growth surface. The thermal evaluation was performed using metallic micro-strip heaters. Two experimental methods were used to achieve this task: (1) direct measurement of the heater temperature as determined from their temperature-dependent characteristics and (2) thermal imaging by using an IR-CCD camera. A comparison of the thermal management properties of SOD, Si and SOI wafers shows that SOD wafers, show significantly better handling of thermal loads than Si or SOI wafers. Even for the Si device layer on the nucleation side of the diamond film, the heat dissipation capacity of the SOD wafers was more than ten times better than that of SOI wafers. The theoretical assessment was performed by finite element modeling and was in good agreement with experimental observations. The analysis showed that the limiting performance factor of the SOD wafers was a relatively thick (1.5 μm) Si device layer used in these studies; even better performance could be obtained by optimizing the SOD structure by making the Si device layer thinner. Following the validation of the primary benefit of SOD, namely its superior thermal management properties, the second task is to assess its electrical properties. The analysis of the interfacial properties between the Si-device layer and diamond is of particular importance. To asses these properties Schottky and pn diodes were fabricated on SOD and SOI wafers. Notably, the diamond-Si interface did not show any trapped charge and no significant difference in the device performance on the two types of wafers was observed. We have demonstrated that SOD technology offers significant thermal management advantages over both SOI and bulk silicon substrates while offering similar electrical characteristics of the Si device layer.