586b Directed Self Assembly of Si and Ge Nanocrystals on Hfo$_2$ through Kinetically Driven Patterning

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The problems created in scaling down microelectronic devices require novel device architectures and material solutions. Two solutions have been proposed to address issues in flash memory devices; first, the continuous floating gate is replaced by an array of nanocrystals that serve as discrete charge storage elements. Faster and more reliable devices are obtained using a nanocrystals based architecture and nanocrystals may be grown in a clean and industry-compatible manner through chemical vapor deposition (CVD). A second solution involves switching to new materials. High-k dielectrics (such as HfO_2) are replacing SiO_2 as the tunnel oxide material in order to address issues of capacitance in the gate area of the device. Additionally, Ge and other new materials are being substituted in place of Si nanocrystals to further refine device characteristics through band gap engineering. However, obstacles remain in scaling down nanocrystal flash memory devices. As devices shrink further, the precise number of nanocrystals within the gate area and their specific arrangement will become reliability issues. A method is needed to controllably deposit nanoparticles within the HfO_2 gate area. In this work, we demonstrate a kinetically-driven patterning scheme for directed self assembly of Si or Ge nanoparticles on HfO_2 regions. This process hinges on the different ways that Ge or Si surface species etch SiO_2 and HfO_2 surfaces, which we have studied with temperature programmed desorption (TPD) and X-ray photoelectron spectroscopy (XPS). This etching depletes the adatom population and hinders self assembly of nanoparticles on the surface. Through judicious choice of growth conditions, we can control which reactions occur in order to limit etching on HfO_2 thereby allowing self assembly of nanocrystals on HfO_2; simultaneously, etching on SiO_2 may be enhanced, effectively preventing self assembly on SiO_2 regions. In this manner, high density arrays ($>3\text{x}10^{11}$ cm^{-2}) of Ge and Si nanocrystals are self assembled in lithographically defined HfO_2 windows using a SiO_2 sacrificial mask. These high density nanocrystal arrays are imaged with scanning electron microscopy (SEM) and atomic force microscopy (AFM). The interactions of Ge and Si with SiO_2 and HfO_2 will be reviewed and explained and the kinetically driven patterning scheme will be demonstrated. Differing issues in creating high density arrays of Si or Ge nanocrystals with CVD will be discussed. This kinetically driven patterning scheme is promising for gate level patterning of nanoparticle arrays.