570d Towards a Co-Design Implementation of a System for Model Predictive Control

Panagiotis Vouzis, Leonidas G. Bleris, Mayuresh V. Kothare, and Mark Arnold

Traditional control techniques face limitations when applied to novel technological applications that are characterized by increased complexity. As an example in biomedical applications, such as active implantable devices, a violation of constraints or a failure to meet control objectives can threaten human life. Model Predictive Control (MPC) appears to be a suitable choice for many of these problems [1]. MPC relies on solving computationally optimization problems characterized by abundant matrix operations with the complexity of the operations increasing considerably with the size of the parameters involved. In this work we provide a framework for the development of low-power and small-chip area real-time MPC implementations, based on codesign analysis, i.e., the cooperative design of hardware and software to achieve the most efficient system. Notably, embedded MPC can be used for numerous areas including biomedical, automotive, robotics or aeronautic applications.

A higher level analysis of the MPC optimization code used reveals that the operations consist mostly of repetitive matrix operations; these comprise the major part of the processing. Clearly, the matrix operations are the main part that has to be implemented efficiently, while the rest of the operations can be performed by a general purpose microprocessor. A solution to this problem can be given using a limited precision host microcontroller together with a matrix processor that acts as a hardware accelerator for the matrix operations. Towards this direction, we propose a codesign step before the actual implementation that decomposes the algorithm into two parts. One that fits into the host processor, which is not required to demonstrate increased accuracy, and one that fits into the custom made unit that performs all the arithmetic operations. Although, the use only of a microprocessor can accommodate the processing load of a MPC algorithm [2], the proposed approach results in improved performance.

The host microcontroller bears the load of performing higher level operations of the algorithm, while the matrix processor the computationally intensive ones. The matrix processor does not have to deal with fetching instructions—the host sends commands and data. For this purpose a command set specially for matrix operations is developed and implemented in a Hardware Description Language (HDL). Since performed experiments indicate that a 16-bit Logarithmic Number System (LNS) unit is adequate for MPC [3, 4], we selected the 16-bit Extensible Instruction Set Controller (EISC) from ADCUS, Inc as the host. For prototyping purposes, we use the 12MHz EISC board, which provides adequate bits of I/O, that we can interface to a 40MHz Xilinx Spartan II Field Programmable Gate Array (FPGA) that acts as the prototype platform for the matrix processor. The current hardware layout is comprised by two different boards, one that accommodates the host and one the FPGA, that communicate via a 20 bit bus (a 16-bit databus and 4 control signals). Since both the host and the coprocessor are described in Verilog, they can both be synthesized to fit in a single FPGA at a later stage. The step before a final fabrication of an Applications-Specific Integrated Circuit (ASIC) that will offer higher performance with lower power consumption and smaller die area.

Consequently, the characteristics of the implementation of a hardware-software design capable of performing all the operations of an MPC algorithm, including chip area, I/O and memory requirements, and the system's performance, will be presented. Additionally, focus will be put on the design steps of the co-design process, as well as on the tools and the arithmetic system used.

[1] R. S. Parker, F. J. Doyle III, N. A. Peppas, “The Intravenous Route to Blood Glucose Control,” IEEE Engineering in Medicine and Biology Magazine, Vol. 20, No. 1, pp. 65 – 73 (Jan./Feb. 2001).

[2] Bleris, L. G. and M. V. Kothare, “Real-Time Implementation of Model Predictive control,” American Control Conference, Portland, OR, June 2005.

[3] J. Garcia, M. G. Arnold, L. Bleris and M. V. Kothare, “LNS Architectures for Embedded Model Predictive Control Processors,” Proc. 2004 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Washington DC, pp. 79-84, Sept. 2004.

[4] L. G. Bleris, J. Garcia, M. V. Kothare and M. G. Arnold, “Towards Embedded Model Predictive Control for System-On-a-Chip Applications,” to appear: Journal of Process Control.