Fault detection and estimation of wafer warpage profile during thermal processing in microlithography

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Keywords: Semiconductor Manufacturing, Microlithography, Fault Detection, Photoresist Processing.

Abstract

Wafer warpage is common in microelectronics processing. Warped wafers can affect device performance, reliability and linewidth control in various processing steps. We proposed in this paper an in-situ approach for estimating wafer warpage profile during the thermal processing steps in microlithography process. A programmable multizone thermal processing system is developed to demonstrate the approach. Early detection will minimize cost and processing time. Based on first principle thermal modeling and system identification techniques, we are able to estimate the profile of a warped wafer from available temperature measurements. Experimental results demonstrate the feasibility and repeatability of the approach. The proposed approach is applicable to other semiconductor substrates.

1 Introduction

Wafer warpage can affect device performance, reliability and linewidth or critical dimension (CD) control in various microelectronic manufacturing processes. The drive toward smaller device geometries has placed much tighter control limits on the various semiconductor manufacturing processes. The reduction in exposure wavelength to create smaller features comes at a higher cost of lower depth of focus. Figure 1 shows a typical microlithography sequence. In the exposure step a warped wafer results in a non-uniform gap between wafer and mask for a contact aligner and different depth-of-focus at different parts of the wafer for a projection exposure system. The significance of having a wafer of minimal warpage is that it makes possible the reduction of the depth-of-focus to achieve a higher pattern resolution [1]. Hence, any knowledge of the wafer warpage profile could act as a source for active compensation during the exposure step in lithography.

Warped wafers also affect the various baking steps in the microlithography sequence [2] shown in Figure 1. Warpage can result in a non-uniform wafer temperature distribution across the wafer. Simulation results show that warpage of less than 50 μm can lead to a temperature variation of 1°C across the wafer during baking [3]. This can lead to substantial spatial variation in CD. Temperature uniformity control is thus an important issue in photoresist processing with stringent specifications [4]. The most important or temperature sensitive step is post-exposure bake. Requirements call for temperature to be controlled within 0.1°C at temperatures between 70°C and 150°C. For commercially available deep ultra violet resist, a representative post-exposure bake latitude for CD variation is about 5 nm/°C [5]. A number of recent investigations also showed the importance of proper bakeplate operation on linewidth or CD control [2], [6]–[10]. Warpage becomes more problematic for larger wafers and the maximum allowable warpage for a 300 mm wafer is 100 μm from center to edge [12].

Current techniques for measuring wafer warpage include capacitive measurement probe [14], shadow Moire technique [15], and pneumatic-electro-mechanical technique [16]. These are off-line method where the wafer has to be removed from the processing equipment and placed in the metrology tool resulting in increase processing steps, time and cost. We have previously demonstrated that by monitoring the bake-plate temperature profile during the thermal processing steps in microlithography, we are able to detect wafer warpages [17]. In this paper, we extend the approach to estimating the profile of the warped wafer. A distributed thermal processing system is developed consisting of an array of heating zones. Each of the zones are separated by a small air-gap of approximately 50 mils. The zones can be controlled independently with separate temperature sensing, actuation and feedback control mechanisms. By monitoring the temperature profiles within each of the heating zones, coupled with first principle thermal modeling and system identification techniques, an estimate of the profile of the warped wafer can be obtained. The proposed approach is also robust to modeling errors compared to our previous method [17] where only a single point (the maximum temperature drop point of the bakeplate) on the plate temperature profile is used for warpage detection.

This paper is organised as follows. A brief outline of the proposed thermal processing system is described in section 2. In Section 3, we develop the model required for predicting warpage profile. Experimental results are given in Section 4 to demonstrate the proposed method. Finally, conclusions are given in Section 5.

2 Thermal Processes in Microlithography

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bakeplate for a given period of time. The heated bakeplate is usually of large thermal mass (see Figure 2) and is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bakeplate near the surface. The wafers are usually placed on proximity pins of the order of 100 to 200 μm to create an air-gap so that the bakeplate will not contaminate the wafers. As wafers can warp up to 100 μm from center to edge, the percentage change in the air-gap between the wafer and bakeplate can be substantial (see Figure 3) resulting in a non-insignificant variation in the bakeplate temperature. When a wafer at room temperature is placed on the bakeplate, the temperature of the bakeplate drops at first but recovers gradually because of closed-loop control (see Figure 4). It is clear that different air-gap sizes will results in different temperature drops in the bakeplate. Since the bakeplate temperature measurements are readily available, detection of wafer warpage is now made possible. We note that this is an in-situ approach compared to conventional off-line methods discussed earlier. For conventional thermal processing system, the proposed approach will provide the user with the information on the degree of warpage; information on the profile of the warpage is not possible due to the fact that the bakeplate is of single zone. To estimate the profile of the wafer, multiple temperature measurement of the bakeplate is required, this is only possible with a multizone bakeplate with integrated temperature sensing within each zone.

2.1 A Distributed Thermal Processing System

In this work, a programmable thermal processing module is developed to provide in-situ estimation of the warped wafer profile. The proposed system also addresses the limitation of conventional bake systems. It is comprised of an array of heating zones that allow for spatial control of temperature in non-symmetric configurations. A resistive heating element is embedded within each of the heating zones. Each heating zone is configured with its own temperature sensor and electronics for feedback control. Each heating zones are separated with a small air-gap of approximately $50\ mils$. The fact that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability. Its small thermal mass allows for fast dynamic manipulation of temperature profile. Depending on application, the number of zones of the bakeplate can be easily configured. Figure 5 shows the prototype multizone system. To estimate the profile of the warped wafer, a thermal model of the system is next developed.

3 Thermal Modeling of the Baking Process

In this section, we present the model for the baking process which will be used subsequently for the estimation of the wafer warpage profile. Analysis of the thermal processing system can be done with a model considering radial as well as the axial effects of heat transfer in the module. Consider the setup of Figure 6, which deals with the plate-airgap-wafer system of a simplified 2-zone system (model for N-zone can be extended easily). The bakeplate is a multizone bakeplate with a small proximity air-gap between each zone. The system is discretized spatially into N radial elements where N corresponds to

the number of zones in the bakeplate. Spatial distributions of temperature and other quantities in a silicon wafer is most naturally expressed in a cylindrical coordinate system. We will assume that the substrate used for baking is a silicon wafer and the bakeplate is cylindrical in shape with the same diameter as the wafer. Energy balances on the wafer and bakeplate can then be carried out to obtain a two dimensional model as follows.

$$C_{p1}\dot{\theta}_{p1} = -\frac{\theta_{p1}-\theta_{p2}}{R_{p1}} - \frac{\theta_{p1}-\theta_{w1}}{R_{a1}} + q_1, \tag{1}$$

$$C_{pi}\dot{\theta}_{pi} = \frac{\theta_{p(i-1)}-\theta_{pi}}{R_{p(i-1)}} - \frac{\theta_{pi}-\theta_{p(i+1)}}{R_{pi}} - \frac{\theta_{pi}-\theta_{wi}}{R_{ai}} + q_i, \qquad 2 \le i \le N-1, \tag{2}$$

$$C_{pN}\dot{\theta}_{pN} = \frac{\theta_{p(N-1)}-\theta_{pN}}{R_{p(N-1)}} - \frac{\theta_{pN}}{R_{pN}} - \frac{\theta_{pN}-\theta_{wN}}{R_{aN}} + q_N, \tag{3}$$

$$C_{w1}\dot{\theta}_{w1} = \frac{\theta_{p1}-\theta_{w1}}{R_{a1}} - \frac{\theta_{w1}-\theta_{w2}}{R_{w1}} - \frac{\theta_{w1}}{R_{wz1}}, \tag{4}$$

$$C_{wi}\dot{\theta}_{wi} = \frac{\theta_{w(i-1)}-\theta_{wi}}{R_{w(i-1)}} + \frac{\theta_{pi}-\theta_{wi}}{R_{ai}} - \frac{\theta_{wi}-\theta_{w(i+1)}}{R_{wi}} - \frac{\theta_{wi}}{R_{wzi}} \qquad 2 \le i \le N-1, \tag{5}$$

$$C_{wN}\dot{\theta}_{wN} = \frac{\theta_{w(N-1)}-\theta_{wN}}{R_{w(N-1)}} + \frac{\theta_{pN}-\theta_{wN}}{R_{aN}} - \frac{\theta_{wN}}{R_{wN}} - \frac{\theta_{wN}}{R_{wzN}}. \tag{6}$$

where

$\theta_{pi} = T_{pi} - T_\infty$	:	$i\ th$ plate element temperature above ambient
$\theta_{wi} = T_{wi} - T_\infty$	:	$i\ th$ wafer element temperature above ambient
T_∞	:	ambient temperature
C_{pi}	:	thermal capacitance of $i\ th$ plate element
C_{wi}	:	thermal capacitance of $i\ th$ wafer element
R_{pi}	:	thermal conduction resistance between the $i\ th$ and $i+1\ th$ plate element
R_{wi}	:	thermal conduction resistance between the $i\ th$ and $i+1\ th$ wafer element
R_{wzi}	:	thermal convection loss of the ith wafer element
R_{ai}	:	thermal conduction resistance between the $i\ th$ plate and $i\ th$ wafer element
q_i	:	power into the $i\ th$ plate element

The various thermal resistances and capacitances are given by

$$
\begin{aligned}
R_{pi} &= \frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_a t_p} \quad (K/W) && 1 \le i \le N-1 \\
R_{pN} &= \frac{1}{h(\pi D t_p)} \quad (K/W) \\
R_{wi} &= \frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_w t_w} \quad (K/W) && 1 \le i \le N-1 \\
R_{wN} &= \frac{1}{h(\pi D t_w)} \quad (K/W) \\
R_{wzi} &= \frac{1}{h A_{zi}} \quad (K/W) \\
R_{ai} &= \frac{t_{ai}}{k_a A_{zi}} \quad (K/W) \\
C_{pi} &= \rho_p c_p \left(t_p A_{zi}\right) \quad (J/K) && 1 \le i \le N \\
C_{wi} &= \rho_w c_w \left(t_w A_{zi}\right) \quad (J/K) && 1 \le i \le N \\
A_{zi} &= \pi \Delta_r^2 \left[i^2 - (i-1)^2\right] \quad (m^2) && 1 \le i \le N
\end{aligned}
$$

where A_{zi} is the cross-sectional area of element i normal to the axial heat flow. t_p, t_w are the bakeplate thickness, wafer thickness and t_{ai} are the air-gap between the ith wafer and bakeplate elements. k_a, k_p and k_w are the thermal conductivity of air, bakeplate and wafer respectively. h is the convective heat transfer coefficient. ρ_p and ρ_w are the density of the bakeplate and wafer respectively. c_p and c_w are the specific heat capacity of the bakeplate and wafer respectively. The width of each element is given by $\Delta_r = D/(2N)$.

Equations 1 to 6 can be rearranged into state-space format.

$$
\begin{aligned}
\dot{\theta} = \begin{bmatrix} \dot{\theta}_p \\ \dot{\theta}_w \end{bmatrix} &= \begin{bmatrix} \mathbf{F_{pp}} & \mathbf{F_{pw}} \\ \mathbf{F_{wp}} & \mathbf{F_{ww}} \end{bmatrix} \begin{bmatrix} \theta_p \\ \theta_w \end{bmatrix} + \begin{bmatrix} \mathbf{G_{pp}} \\ \mathbf{0_N} \end{bmatrix} \mathbf{q} \qquad (7) \\
&= \mathbf{F}\theta + \mathbf{G}\mathbf{q},
\end{aligned}
$$

where

$$
\begin{aligned}
\mathbf{F_{pp}}(1,1) &= -\frac{(1/R_{p1}+1/R_{a1})}{C_{p1}}, \\
\mathbf{F_{pp}}(i,i) &= -\frac{\left(1/R_{p(i-1)}+1/R_{pi}+1/R_{ai}\right)}{C_{pi}} \quad 2 \le i \le N, \\
\mathbf{F_{pp}}(i,i+1) &= \frac{1/R_{pi}}{C_{pi}} \quad 1 \le i \le N-1, \\
\mathbf{F_{pp}}(i,i-1) &= \frac{1/R_{p(i-1)}}{C_{pi}} \quad 2 \le i \le N, \\
\mathbf{F_{ww}}(1,1) &= -\frac{(1/R_{w1}+1/R_{a1}+1/R_{wz1})}{C_{w1}}, \\
\mathbf{F_{ww}}(i,i) &= -\frac{\left(1/R_{w(i-1)}+1/R_{wi}+1/R_{ai}+1/R_{wzi}\right)}{Cwi} \quad 2 \le i \le N, \\
\mathbf{F_{ww}}(i,i+1) &= \frac{1/R_{wri}}{C_{wi}} \quad 1 \le i \le N-1, \\
\mathbf{F_{ww}}(i,i-1) &= \frac{1/R_{wr(i-1)}}{C_{wi}} \quad 2 \le i \le N.
\end{aligned}
$$

In addition, $\mathbf{F_{pw}}$ and $\mathbf{F_{wp}}$ are diagonal matrices given by

$$
\mathbf{F_{pw}} = \begin{bmatrix} \frac{1}{R_{a1}C_{p1}} & 0 & \cdots & \\ 0 & \frac{1}{R_{a2}C_{p2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{R_{aN}C_{pN}} \end{bmatrix},
$$

and

$$
\mathbf{F_{wp}} = \begin{bmatrix} \frac{1}{R_{a1}C_{w1}} & 0 & \cdots & \\ 0 & \frac{1}{R_{a2}C_{w2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{R_{aN}C_{wN}} \end{bmatrix}.
$$

The excitation term, $\mathbf{G_{pp}}$ is given by

$$
\mathbf{G_{pp}} = \begin{bmatrix} \frac{1}{C_{p1}} & 0 & \cdots & \\ 0 & \frac{1}{C_{p2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{C_{pN}} \end{bmatrix}.
$$

In the next section, we will demonstrate that by monitoring the bakeplate temperatures, θ_{pi}, and making use of system identification techniques [20], we are able to extract the air-gap information, t_{ai}, between the ith wafer and bakeplate elements. Coupled with the information of the proximity pins, the profile of the warped wafer can be obtained, we demonstrate experimentally the approach on a 2-zone system.

4 Experimental Verification: Estimation of Warpage Profile

Although most of the parameters in the model developed in the previous section can be obtained from handbooks, to obtain a more accurate and realistic model of the actual system, actual input-output data is used to estimate the various parameters in Equation 8. In this section, we will first outline the experimental setup used to estimate the warped wafer profile and the experiments performed to demonstrate the feasibility and repeatability of the proposed approach.

4.1 Experimental Setup

The experimental setup for the baking of 200 mm wafer is shown in Figure 5. As discussed previously, the programmable thermal system can be configured up to N zones. Without loss of generality, we will demonstrate our proposed approach on a 2-zone system. Two proportional-integral (PI) controllers are used respectively to control the two zones of the bakeplate. The PI parameters for the central and external zones are given by $K_{c1} = 14.0$, $T_{i1} = 300$ and $K_{c2} = 45.0$, $T_{i2} = 300$ respectively. The experiments were conducted at a temperature setpoint of 90°C with a sampling and control interval of 0.5 seconds. This temperature corresponds to a soft-bake condition for photoresist processing [21].

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from 15°C to 150°C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks [22]:

density of silicon:	$\rho_w = 2330$ kg/m^3
density of aluminum:	$\rho_p = 2700$ kg/m^3
specific heat capacity of silicon:	$c_w = 0.75$ kJ/kgK
specific heat capacity of aluminum:	$c_p = 0.917$ kJ/kgK
thermal conductivity of air:	$k_a =$0.03 W/mK
thermal conductivity of silicon:	$k_w = 99$ W/mK
convective heat transfer coefficient:	$h = 3$ W/m^{2}K
thickness of 200 mm wafer:	$l_w =$750 μm

4.2 Initialization Phase

The proposed approach required detailed information of the system in order to identify the airgap during each subsequent processing. As such, certain parameters that do not vary during subsequent processing can be estimated via system identification techniques beforehand. For the 2-zone system, the various

elements of the state-space representation of Equation 8 can be expressed as follows:

$$
\begin{aligned}
F_{pp} &= \begin{bmatrix} -\frac{1}{C_{p1}}(\frac{1}{R_{p1}}+\frac{1}{R_{a1}}) & \frac{1}{C_{p1}}\frac{1}{R_{p1}} \\ \frac{1}{C_{p2}}\frac{1}{R_{p1}} & -\frac{1}{C_{p2}}(\frac{1}{R_{p1}}+\frac{1}{R_{a2}}+\frac{1}{R_{p2}}) \end{bmatrix} \\
F_{pw} &= \begin{bmatrix} \frac{1}{C_{p1}}\frac{1}{R_{a1}} & 0 \\ 0 & \frac{1}{C_{p2}}\frac{1}{R_{a2}} \end{bmatrix} \\
F_{wp} &= \begin{bmatrix} \frac{1}{C_{w1}}\frac{1}{R_{a1}} & 0 \\ 0 & \frac{1}{C_{w2}}\frac{1}{R_{a2}} \end{bmatrix} \\
F_{ww} &= \begin{bmatrix} -\frac{1}{C_{w1}}(\frac{1}{R_{w1}}+\frac{1}{R_{wz1}}+\frac{1}{R_{a1}}) & \frac{1}{C_{w1}}\frac{1}{R_{w1}} \\ \frac{1}{C_{w2}}\frac{1}{R_{w1}} & -\frac{1}{C_{w2}}(\frac{1}{R_{w1}}+\frac{1}{R_{a2}}+\frac{1}{R_{w2}}+\frac{1}{R_{wz2}}) \end{bmatrix} \\
G_{pp} &= \begin{bmatrix} \frac{1}{C_{p1}} & 0 \\ 0 & \frac{1}{C_{p2}} \end{bmatrix}
\end{aligned}
$$

The various thermal capacitances and resistances can then be computed as follow:

$$
\begin{aligned}
A_{z1} &= \pi\Delta r \times \Delta r = 0.0079\text{m}^2 \\
A_{z2} &= \pi(2\Delta r \times 2\Delta r - \Delta r \times \Delta r) = 0.0237\text{m}^2 \\
C_{w1} &= \rho_w V_{w1} c_w = \rho_w (A_{z1} l_w) c_w = 0.0103 \text{ kJ/K} \\
C_{w2} &= \rho_w V_{w2} c_w = \rho_w (A_{z2} l_w) c_w = 0.0309 \text{ kJ/K} \\
R_{wz1} &= \frac{1}{hA_{z1}} = 42.1941\text{K/W} \\
R_{wz2} &= \frac{1}{hA_{z2}} = 14.065\text{K/W} \\
R_{w1} &= \frac{\ln(\frac{1+1/2}{1-1/2})}{2\pi k_w t_w} = 2.3549\text{K/W} \\
R_{w2} &= \frac{1}{h(\pi D t_w)} = 707.36\text{K/W} \\
R_{p1} &= \frac{\ln(\frac{1+1/2}{1-1/2})}{2\pi k_a t_p} = 544.70\text{K/W} \\
R_{p2} &= \frac{1}{h(\pi D t_p)} = 49.581\text{K/W}
\end{aligned}
$$

The rest of the parameters that we do not have full knowledge of are then estimated via system identification techniques. For a given bakeplate, the bakeplate element thermal capacitances (C_{p1} and C_{p2}) are expected to be fixed and hence can be determined during the initialization phase of the experiment. Run(a) in Figure 4 was used to determine the plate element thermal capacitances, C_{p1}, C_{p2} in the state-space matrices. The experiment was conducted by dropping a flat wafer on the bakeplate with a known air-gap of $t_a = 55$ μm. Since the respective airgaps are known (i.e. t_{a1} and t_{a2}), the airgap resistances R_{a1} and R_{a2} can be computed as

$$
\begin{aligned}
R_{a1} &= \frac{t_{a1}}{k_a A_{z1}} = 0.2321\text{K/W} \\
R_{a2} &= \frac{t_{a1}}{k_a A_{z2}} = 0.0774\text{K/W}
\end{aligned}
$$

Next, to determine the unknown parameters C_{p1} and C_{p2} in the structured state-space model in Equation 7, standard state-space identification algorithms [20] can be used. The bakeplate temperature profile of the 2-zone system is then fitted using the structured state-space model. Run(a) in Figure 4 shows the simulation results which was generated using the estimated C_{p1} and C_{p2}. The estiamted parameters are: $C_{p1} = 208 \times 10^{-3} KJ/K$, $C_{p2} = 738 \times 10^{-3} KJ/K$

4.3 Warpage Profile Estimation

Once the various wafer, bakeplate and PID controllers parameters are known, the average airgap (t_{a1} and t_{a2}) in each zones can be estimated via state-space identification using available bakeplate temperature measurements (θ_{p1} and θ_{p2}). The feasibility and repeatability of the approach is demonstrated via a series of experiments.

Experimental runs (b) and (c) in Figure 4 shows the case of the flat wafer dropped on the bakeplate with different proximity pins (i.e. different airgaps). The proximity pin height, l_p for runs (b) and (c) are 110μm and 165μm respectively. The estimated airgaps for the two runs are tabulated in Table 1. A good measure of the extent warpage is to measure the deviation of the average airgap from the proximity pin height. δ_1 and δ_2 in experimental runs (b) and (c) is closed to zero as expected since the wafer is flat.

Experimental runs (d) and (e) in Figure 4 shows the case of a wafer with center-to-edge warpage of 110μm dropped on the bakeplate with different proximity pins height. The proximity pin height, l_p for runs (d) and (e) are 220μm and 165μm respectively. The estimated airgaps for the two runs are also tabulated in Table 1. δ_1 and δ_2 in experimental runs (d) and (e) are approximately the same. Based on the estimated δ_1 and δ_2 together with the proximity pin height, the profile of the wafer can be obtained by extrapolation as shown in Figure 7 (based on experimental run(e)). An estimated warpage of 109.4μm from center-to-edge for the warped wafer is obtained.

These two sets of experimental runs ((b), (c) and (d), (e)) demonstrate the feasibility of the approach in that different bake system might have different proximity pin gaps, however the degree of warpage should be the same for the same wafer. Next, the repeatability of the proposed approach is demonstrated in Figure 8 where the experimental conditions (d) in Table 1 were repeated 10 times. For each run, the data is fitted to the state-space model in Equation 7. In this paper, we have demonstrated that it is possible to estimate the profile of a wafer. We expect accuracy to improve if the number of zones in the bakeplate increased

5 Conclusions

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence. In this paper, we have presented a novel approach to detect and estimate warpage in semiconductor substrates. Based on first principle modeling of the thermal system and by

monitoring the bake-plate temperature during the baking of wafer in microlithography, we are able to detect and estimate the profile of the wafer from available temperature measurements. Experimental results demonstrate the feasibility and repeatability of the approach.

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Expt. run	Proximity pin height l_p (μm)	Estimated air-gap		Deviation from flat wafer	
		center zone t_{a1} (μm)	edge zone t_{a2} (μm)	center zone $\delta_1 = t_{a1} - l_p$ (μm)	edge zone $\delta_2 = t_{a2} - l_p$ (μm)
(b)	110.0	109.0	107.8	-1.0	-2.2
(c)	165.0	162.1	163.7	-2.9	-1.3
(d)	220.0	125.5	174.0	-94.5	-46.0
(e)	165.0	69.1	124.8	-95.9	-41.2

Table 1: Estimation of air-gap.

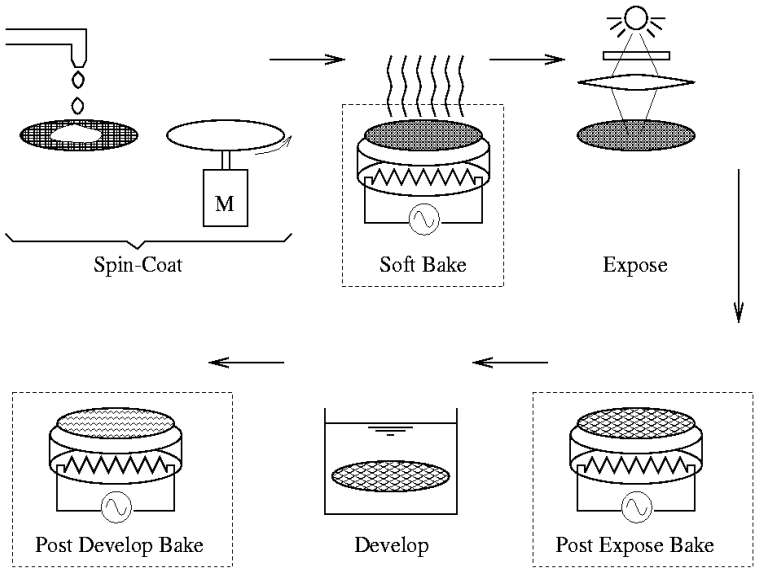

Figure 1: The lithography sequence.

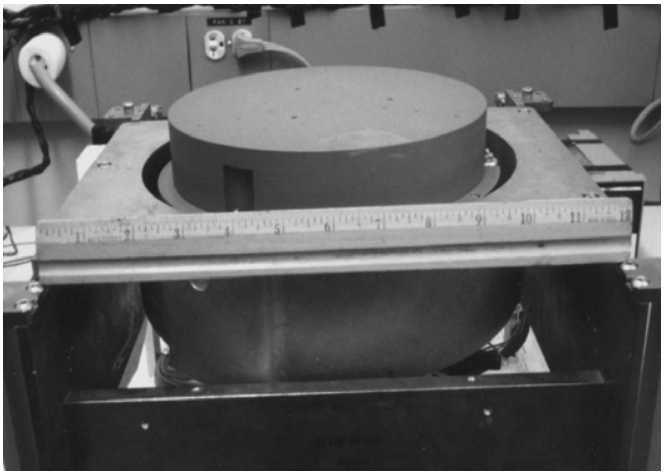

Figure 2: Conventional bake-plate.

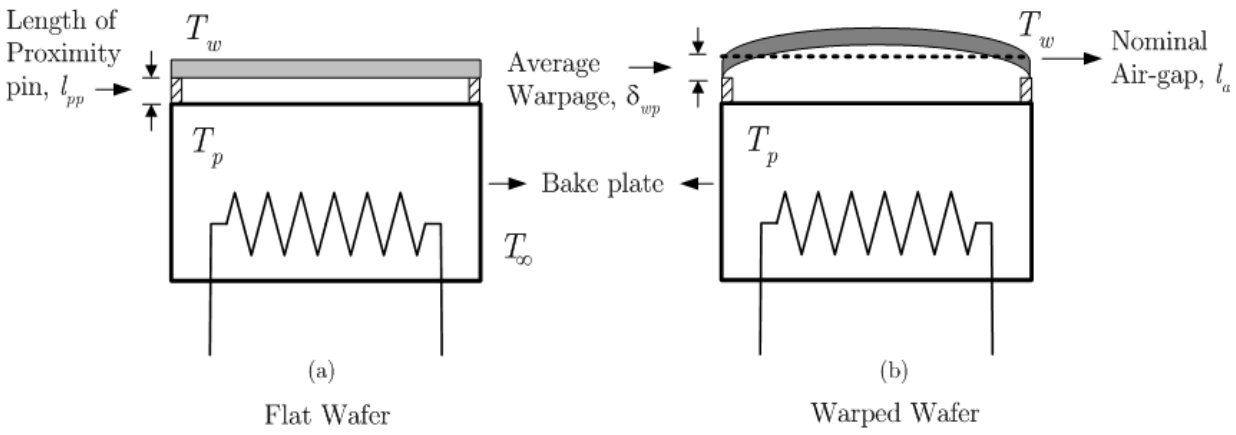

Figure 3: Schematic diagram of the baking process for a flat and warped wafer. Notice the difference between the air-gap of the wafer and bakeplate.

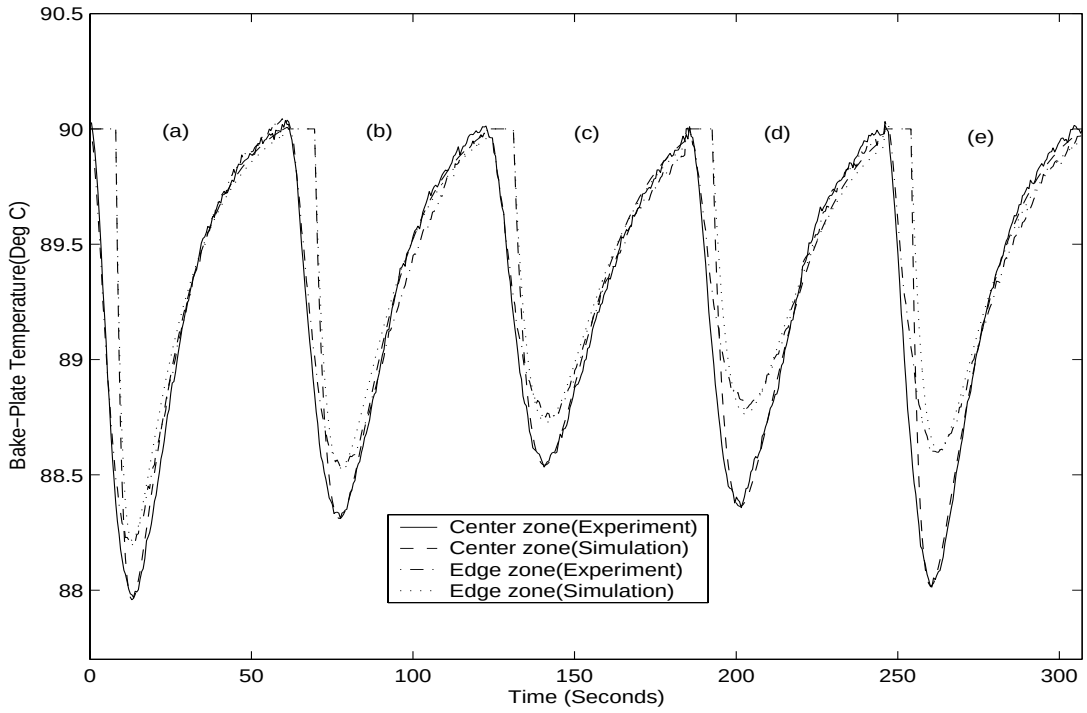

Figure 4: Results for 5 experimental runs to demonstrate that different air-gap sizes cause different magnitudes of temperature drops before recovery for a 2-zone baking system. The solid and dashed curves represent the experimental and simulation result of the bakeplate temperature in center zone respectively; the dash-dotted and dotted curves represent the experimental and simulation result of the bakeplate temperature in edge zone respectively.

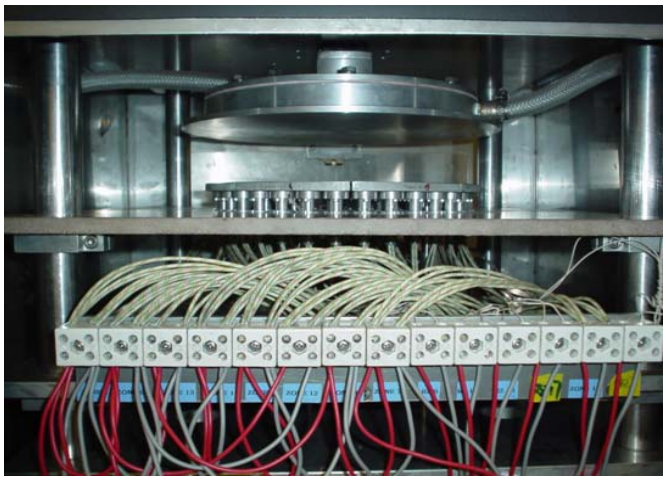

Figure 5: A programmable multizone thermal processing system.

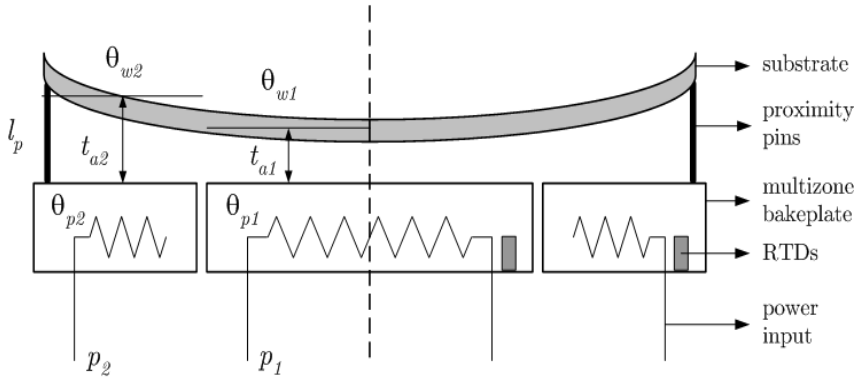

Figure 6: Thermal modeling of a 2-zone thermal processing system.

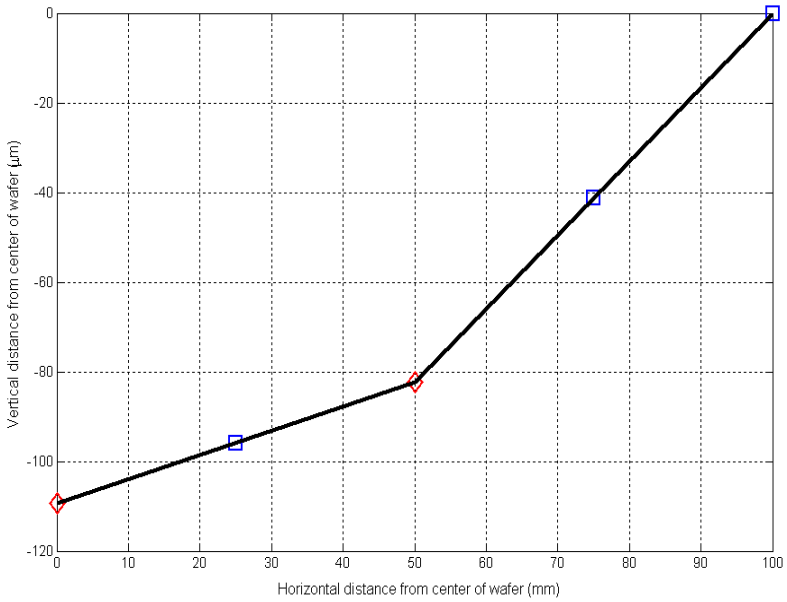

Figure 7: Estimated profile of the warped wafer based on experimental run(e).

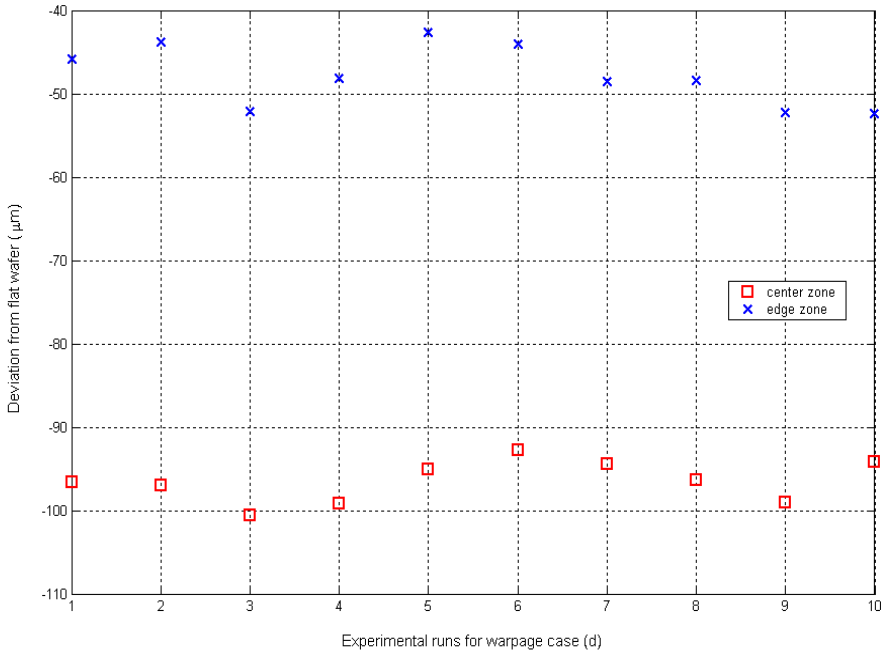

Figure 8: Experimental runs for the warped wafer based on experimental run(d).