In-situ Measurement and Control for Photoresist Processing in Microlithography

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Abstract

The lithography process is the critical step in the fabrication of nanostructures for integrated circuit manufacturing. It accounts for one third of the costs of manufacturing integrated circuits. The rapid transition to smaller microelectronic feature sizes involves the introduction of new lithography technologies, new photoresist materials, and tighter processes specifications. This transition has become increasingly difficult and costly. The application of advanced computational and control methodologies have seen increasing utilization in recent years to improve yields, throughput, and, in some cases, to enable the actual process to print smaller devices. In this paper, we point out applications in the lithography process where systems methods (the use of in-situ measurement and control) have made an impact as well as future challenges in this research. The most important variable to control in the lithography process is the linewidth or critical dimension (CD), which perhaps is the single variable with the most direct impact on the device speed and performance. Our objective is to identify key parameters in the lithography sequence that has an impact on the final critical dimension (CD).

1 Introduction

Lithography is the key enabler and “bottleneck” controlling the device scaling, circuit performance and magnitude of integration for silicon semiconductors. This integration drives the size, weight, cost, reliability and capability of electronic systems. The lithography process accounts for 30-35% of the costs of manufacturing integrated circuits. The rapid transition to smaller microelectronic feature sizes involves the introduction of new lithography technologies, new photoresist materials, and tighter processes specifications. This transition has become increasingly difficult and costly. The application of advanced computational and control methodologies have seen increasing utilization in recent years to improve yields, throughput, and, in some cases, to enable the actual process to print smaller devices [1, 2, 3]. The value of applying such mathematical systems science tools to microelectronics manufacturing has already been demonstrated in the area of photoresist thermal processing [3, 4, 5, 6, 7, 8, 9], rapid thermal processing [10, 11, 12] and plasma processing [13, 14]. The recent report of the international panel on future directions in control, dynamics and systems [15] has also identified control as critical to future progress in the semiconductor sectors. Modeling plays a crucial role and control techniques must make use of increase in-situ measurements to control at a variety of temporal and spatial scales.

In this paper, we point out applications in the lithography process where systems methods have made an impact. For example, with the introduction of chemically amplified photoresists, the temperature sensitivity of the post-exposure thermal process is now significant. Poor nonuniformity directly impacts the linewidth distribution and the chip performance. With linewidths decreasing below 100 nm, there is a need to minimize temperature variations and maximize process robustness for thermal processing of resists, otherwise a significant portion of the process error budget will be consumed. Although less temperature sensitive photoresist materials are desired, the requirements become more stringent as the feature size shrinks. Hence, the temperature uniformity specifications remain important even though new materials are invented. Consequently, the temperature control system for this process requires careful consideration, including the equipment design and temperature sensing techniques.

Figure 1 depicts the typical steps in a lithography process [16]. In addition to the exposure step, lithography requires precise processing of the photoresist. This sequence of operations begins with a priming step to promote adhesion of the polymer photoresist material to the substrate. A thin layer (typically one micron) of resist is spin-coated on the wafer surface. The solvent is evaporated from the resist by a baking process. After patterning with (deep UV) radiation, a post-exposure bake process is used to promote a reaction that alters the solubility of the resist in the exposed areas. A subsequent chemical develop step then removes the exposed/reacted resist material while keeping the non-exposed areas in place. The developed resist is then baked to promote etching stability. The most important variable to control in the lithography process is the linewidth or critical dimension (CD), which perhaps is the single variable with the most direct impact on the device speed and performance. Our objective is to identify key parameters in the lithography sequence that has an impact on the final CD.

This paper is organized as follows. In section 2, a case study is presented for the design and implementation of a control system for a novel bake/chill system used to achieve temperature control of acid catalyzed photoresists. This case study demonstrates the need to consider the limitations imposed by the equipment design on the ultimate performance of the control system. In Section 3, we present an innovative method to control the photoresist thickness uniformity. In section 4, conclusions are presented to assess the future application of advanced systems techniques to the lithography process.

2 Multizone Integrated Bake/Chill System

Each step within the resist processing sequence must achieve stringent performance requirements to minimize variations to the CD distribution. This has been accomplished by robust design of the equipment and process for repeatable operation. Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated plate for a given period of time followed by a chilled step. The heated plate is of large thermal mass relative to the wafer and is held at a constant temperature by a feedback controller that adjusts the resistive heater power in response to a temperature sensor embedded in the plate near the surface. These bake systems do not have the capability of measuring the substrate temperature. Current approaches typically make used of an instrumented wafer [17], which has embedded sensors and wires running to the instrumentation, enabling measurements across the substrate. However, these methods run into difficultly when implemented in an environment where the “hotplates” are encapsulated with a lid on them. A wireless version of such instrumented wafer do exist [18], however both approaches are typically used at the initial characterization phase for determining the optimum recipes since the actual substrates do not have embedded sensors. During the subsequent runs, the process is subjected to process drifts and disturbances (e.g. wafers of different warpages); with in-situ temperature measurement, we can correct for these changes in the process easily. Also, with sensor-based control, expenses in traditional maintenance schedules for equipment can be minimized. Although these conventional photoresist processing technologies have preformed remarkably well, there is a need to improve the productivity of these operations including narrowing the CD distribution, improving throughput and reducing set-up times. Our objective is thus to develop a new thermal system with in-situ temperature measurement system capable of implementing advanced process control which is fast becoming a necessity for next generation of photoresist processing.

First, the PEB step is especially sensitive to temperature variation calling for precise temperature control [19, 20, 21]. There are several areas where the performance of bake and chill plates can be improved. A number of recent investigations also show the importance of proper bake plate operation on CD control [22, 23]. For example, temperature nonuniformities during transients, including ramp-up and the movement of the substrate between the bake and chill plates, need to be minimized to narrow the CD distribution. To improve the transient and spatial control of the bake and chill plates a new approach to the design is needed. The reason is that the large thermal mass of the conventional hot plates prevents rapid movements in substrate temperature to compensate for real-time errors during transients. The implementation of advanced control systems with conventional technology cannot overcome the inherent operating limitations. We investigated this problem of PEB temperature control. Our approach was to modify the conventional technology so that the temperature nonuniformities during the transients could be controlled. This required consideration of the dynamics involved in wafer heating, as well as practical material and operating issues to achieve repeatable and sustained operations. In addition, to improve the quality and throughput of the microlithography process, one way is to incorporate several steps such as baking, chilling and spinning into an integrated system. The overall process time can be reduced if temperature can be controlled as the wafer is being spun at different speeds in readiness for the next step.

Figure 3 shows the proposed thermal processing system. The system integrates the baking and chilling steps into a single module, this eliminate undesirable temperature fluctuations and an uncontrolled situation due to substrate movement. The heater module is comprised of an array of heating zones that allow for spatial control of temperature in non-symmetric configurations. Each of the heating zones is

separated by an air-gap of approximately 200 μm. A resistive heating element is embedded within each of the heating zones. Each heating zone is configured with its own temperature sensor and electronics for feedback control. Multivariable feedback control algorithms are used to manipulate the heating zones to the desired substrate temperature profile. A chill plate circulating water is used to remove heat from the base plate, and the connected heating elements. The system also provides in-situ sensing of the substrate temperature. During baking, the substrates rest on proximity pins which has temperature sensors embedded in it. Real-time closed-loop control of the substrate temperature is thus possible as oppose to conventional open-loop control of the substrate temperature. Figure 4 shows the control of a 200 mm silicon wafer using the in-situ sensors, a multivariable linear quadratic regulator [27] is used to control the 3 temperature points. Note also that the slow ramp rate is due to limitation in electrical input power to about a quarter of the electrical rating of the heaters. The system was however designed with the ability to provide more electrical input power. The temperature uniformity can also be improved further.

There are several processing and manufacturing advantages associated with this improved thermal processing system, including better temperature uniformity control of the substrate during baking compared to conventional systems, throughput improvement due to its lower thermal mass. Another advantage is in rapid design of experiment, to determine the optimal recipes for post-exposure baking, it is normally necessary to obtain data at multiple temperatures. These studies can be time-consuming and costly. In addition, errors can occur if drifts in the other equipment affect results making it difficult to determine the impact that temperature has on the process. Using the spatially-programmable plate, it becomes possible however to achieve several different processing temperatures using a single experiment. This situation is achieved by programming the temperature to different set-points across the surface of the substrate by utilizing the multizone temperature control capability. Figure 5 shows the sensitivity of the linewidth of a quartz photomask to post-apply bake temperature as determined from a single experimental run. A different version of the thermal array for photomask processing was controlled to 49 separate temperature setpoints incremented uniformly within the range of 80 to 140C. The linewidth or CD, in one of the legs of a cross was mapped to the corresponding positional location of the bakeplate temperature. A more detailed description of the results can be found in Schaper et al. [26].

3 Monitoring and Control of Photoresist Film Properties

As discussed in the earlier sections, critical dimension (CD) or linewidth is one the most critical variable in the lithography process with the most direct impact on the device speed and performance of integrated circuit. One exciting new challenge for process control is the development of control and optimization strategies that compensate for the non-uniform processing in one step (process) with that in another. An effective controller could work to resolve several integration problems, possibly speeding development time. In the next few sections, we will describe a number of innovative approaches to controlling the various photoresist properties that can have an impact on the CD uniformity.

In the softbake step, the key parameters that affect the CD are the photoresist thickness and photoresist absorption coefficient. Spatial and temporal control of photoresist thickness has been previously addressed [8]. In this section, the focus is on the control of the photoresist absorption coefficient. The absorption coefficient determined the required exposure dose for printing the features. Hence, nonuniformity in absorption coefficient across the substrate will lead to nonuniformity in the linewidth. Any

variation in the absorption coefficient due to the spin-coating process can be compensated in the softbake step. It is interesting to note that previous works in the literature can only control the average uniformity of the absorption coefficient [9, 30]. The chemical properties of the photoresist consist of the film's index of refraction n, and absorption coefficient k. The absorption coefficient of the photoresist depends on the photoactive compound concentration, PAC, inside the resist and Dill's A, B, and C parameters [30]

$$k = \lambda \frac{A(\lambda) \times \mathrm{P}AC + B(\lambda)}{4\pi} \tag{1}$$

where λ is the light wavelength, $A(\lambda)$ is the net absorption of the inhibitor, and $B(\lambda)$, the net absorption of the base resin. During softbake, Dill's A, B parameters are functions of both the bake temperature and time [31]; since exact parameters of A, and B is not available, an exact value of PAC is difficult to obtain. However, from equation 1, it is clear that controlling the absorption coefficient, k is equivalent to controlling the PAC. The absorption coefficient is not only related to PAC, it is also influenced by the resist thickness due to the thin-film interference. A graph of resist sensitivity versus thickness will show a regular pattern of oscillations, often referred to as the swing curve. Because of the direct relationship between resist sensitivity and linewidth, it is important to control the resist sensitivity to reach an extremum in the swing curve. So the absorption coefficient of the resist has to be well controlled to remain at the extremum of the swing curve [28]. In the next section, we present the spatial control of the photoresist absorption coefficient during the softbake process using the multizone thermal system developed earlier and an array of in-situ spectrometers.

Photoresist development is another one of the steps in microlithography that can have an impact on the CD uniformity. The parameters that are expected to be critical in the development step are temperature and developer concentration. Nonuniformity in the time to reach endpoint can cause nonuniformity in the linewidth. In this paper, we present an innovative approach to control the development process in real-time by monitoring the photoresist thickness during the development process. Using the proposed approach, the time to reach end-point is repeatable from wafer to wafer.

3.1 Monitoring Photoresist Flim Properties

Figure 3 shows the experimental setup for monitoring the photoresist film properties in real-time using in-situ spectrometers. An array of in-situ sensors is positioned above the wafer to monitor the resist thickness and absorption coefficient as shown in Figure 3. The in-situ thickness measurements is also used to detect the endpoint of the development process. The setup comprises a broadband light source (LS-1), a spectrometer with the capability of monitoring the reflected light intensity at three sites simultaneously (SQ2000) and a bifurcated fiber optics reflection probe (R200) from OceanOptics [32]. The reflection probe consisting of a bundle of 7 optical fibers (6 illumination fibers around 1 read fiber) is positioned above the wafer to monitor the resist thickness in real-time. During the softbake and development steps, light from the broadband light source is focused on the resist through one end of the probe and the reflected light is guided back to the spectrometer through the other end.

For the system, reflectance signals in the wavelength range from 350 nm to 900 nm can be obtained. At higher wavelength, the photoresist absorption of light is very close to zero. Therefore, the photoactive compound in the photoresist will not alter the reflectance of light at this range of wavelengths. So the thickness can be calculated using the higher wavelengths reflectance signals. Once the photoresist

thickness is obtained, the absorption coefficient k can be derived from the shorter wavelengths. For Shipley 1813 photoresist, which is a positive g-line photoresist, the wavelength range of 421-450 nm is used to estimate the absorption coefficient k.

Consider an absorbing photoresist film with a complex index of refraction of $n_r + ik$. Its relation with the reflectance intensity is give by [33]:

$$h(\lambda, k) = \frac{\rho_{12}^2 e^{2k\eta} + \rho_{23}^2 e^{-2k\eta} + 2\rho_{12}\rho_{23} cos(\phi_{23} - \phi_{12} + 2n_r\eta)}{e^{2k\eta} + \rho_{12}^2\rho_{23}^2 e^{-2k\eta} + 2\rho_{12}\rho_{23} cos(\phi_{23} + \phi_{12} + 2n_r\eta)} \tag{2}$$

where

$$\rho_{12} = \frac{(n_a - n_r)^2 + k^2}{(n_a + n_r)^2 + k^2} \quad \rho_{23} = \frac{(n_s - n_r)^2 + k^2}{(n_s + n_r)^2 + k^2} \quad \phi_{12} = arctan\frac{2k}{n_r^2 + k^2 + 1} \quad \phi_{23} = arctan\frac{2kn_s}{n_r^2 + k^2 - n_s^2}$$
$$\eta = \frac{2\pi}{\lambda} y$$

and n_a, n_r and n_s are the refractive index of air, resist, and substrate, respectively. y is the resist thickness. The variation of the resist refractive index with wavelength λ is given by the Cauthy equation [33]

$$n_r(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{3}$$

where A, B, C are the Cauchy parameters of the resist and for the case of Shipley 1813 photoresist A = 1.5935, B = 1.8854$\times 10^4$, and C = 4.1211$\times 10^6$.

Given the reflectance measurements, the resist absorption coefficient can be estimated using equation 2. The solution to the problem is non-convex and does not contain a global minimum over the search space. However, we have a reasonably good initial estimate of the resist thickness from the coating process. Therefore, a local minimum solution for the resist thickness is obtained using least square estimation. To do this, equation 2 is approximated by taking the Taylor series expansion such that

$$h(\lambda, k) = h(\lambda, k_0) + \frac{\partial h}{\partial k}|_{\lambda, k_0} \delta k$$

where k_0 is the initial coefficient estimate and $\partial h / \partial k$ the derivative. The estimated absorption coefficient is then given as

$$\hat{k} = k_0 + \delta k$$

and the change in absorption coefficient δk is estimated using the least square method given by

$$\delta k = (\frac{\partial h}{\partial k}^T \frac{\partial h}{\partial k})^{-1} \frac{\partial h}{\partial k}^T (k - k_0)$$

where

$$\frac{\partial h}{\partial k} = \begin{bmatrix} \frac{\partial h}{\partial k}|_{\lambda_1, k_0} \\ \frac{\partial h}{\partial k}|_{\lambda_2, k_0} \\ ... \\ \frac{\partial h}{\partial k}|_{\lambda_M, k_0} \end{bmatrix} \quad h = \begin{bmatrix} h(\lambda_1, k) \\ h(\lambda_2, k) \\ ... \\ h(\lambda_M, k) \end{bmatrix} \quad h_0 = \begin{bmatrix} h(\lambda_1, k_0) \\ h(\lambda_2, k_0) \\ ... \\ h(\lambda_M, k_0) \end{bmatrix}$$

To estimate the absorption coefficient, reflectance measurements (M = 81) are obtained at wavelength between 421-450 nm, about 0.36 nm apart. A sample period of 1 s is selected. The initial estimated k_0 is updated with the current value of $\hat{k}$ at every sample. For the development process, the same set of equations can be used except that only the resist thickness is required and instead of using the refractive index of air, the refractive index of developer solution is used in equation 2.

3.2 Control of Photoresist Absorption Coefficient Uniformity

Our approach to controlling the resist absorption coefficient uniformity uses an array of in-situ spectrometers positioned above the multizone bakeplate to monitor the resist thickness as discribed in the previous section. With these in-situ measurements, the temperature profile of the bakeplate is controlled in real-time by manipulating the heater power distribution using a standard PI controller. The sampling rate is 1 second. Absorption coefficient non-uniformity of less than 3% at a specified target thickness may be achieved. Various sites on the wafer are made to follow a predefined absorption coefficient trajectory to reduce non-uniformity to less than 3% at endpoint.

Table 1 shows 9 experimental runs of the soft-baking process. Runs $1-3$ were conducted using conventional softbake while Runs $4-9$ were conducted using the novel setup. For Runs $1-3$, temperatures at two sites were maintained at $90^{\circ}C$. Throughout the softbake process, the absorption coefficient non-uniformity was measured. Figure 6 shows the experimental result of Run 1. The initial absorption coefficient non-uniformity at about 20 seconds was 0.0012 and final absorption non-uniformity at 300s was about 0.002.

The result of experiment Run 5 is shown in Figure 7. Absorption coefficient at two sites were monitored and made to follow a predefined reference trajectory. The initial absorption coefficient non-uniformity at about 20 seconds was 0.0015 and final absorption non-uniformity at 300s was about 0.001. Even after the absorption coefficient at the two sites converge to the target, absorption coefficient non-uniformity was maintained. The results demonstrate that we are able to reduce the absorption coefficient non-uniformity across individual wafer as well as from wafer-to-wafer with good repeatability. The approach can be extended to more points as necessary.

3.3 Real-time Control of Photoresist Development Process

To control the resist development process, we proposed to conduct the development step using the same setup as the softbake step. A droplet of developer is then dropped on the site where film thickness is monitored. This is to emulate the common used puddle develop method. To demonstrate the control strategy, the decreasing film thickness at that site is monitored and controlled to track a reference thickness profile. A simple PI controller is then used to manipulate the heater power to control the development rate. Figure 8 shows the experimental results. Run 1 and 2 in dash-dotted and dotted line demonstrate real-time control of the development process to follow a reference trajectory and repeatability of the proposed approach. The "$\diamondsuit$" and "+" corresponds to conventional development process with the developer at different temperature. The next phase of the research involves demonstrating the approach in controlling the development process uniformity within the wafer.

4 Conclusions

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence. In this paper, we have pointed out a few areas where systems techniques have played a significant role in improving the lithograph process. These areas include thermal system design and the use of advanced control and signal processing techniques to improve the photoresist absorption coefficient uniformity and real-time control of the photoresist development process.

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Bake Approach	Conventional Bake			Multizone-PI					
Run Number	1	2	3	4	5	6	7	8	9
Nonuniformity after 20s	0.0012	0.0015	0.0011	0.0012	0.0015	0.0013	0.0027	0.0013	0.0019
Nonuniformity after 100s	0.0028	0.0031	0.0027	0.0006	0.0009	0.0004	0.0009	0.0010	0.0008

Table 1: Summary of experimental runs. The first 3 runs are for standard softbake, the last 7 runs using the proposed approach.

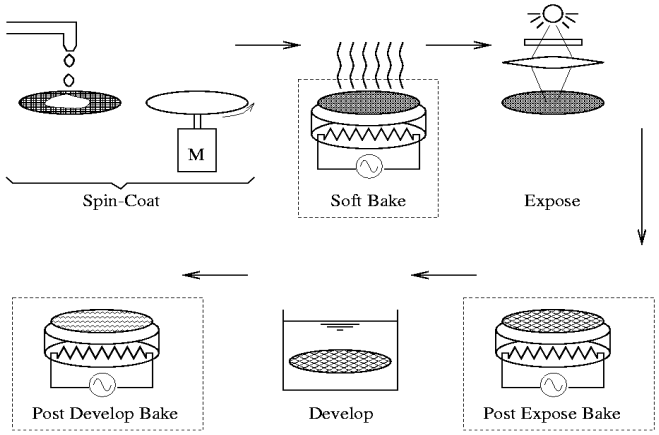

Figure 1: The lithography sequence.

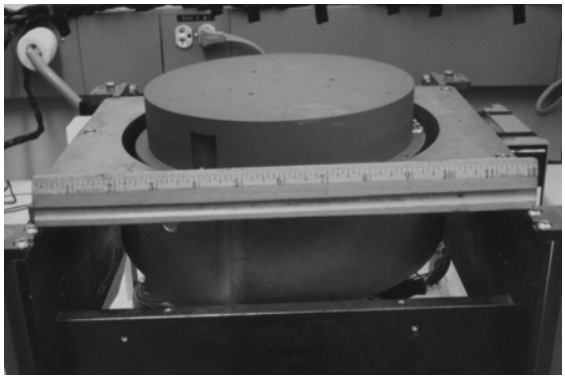

Figure 2: Commercial bake-plate.

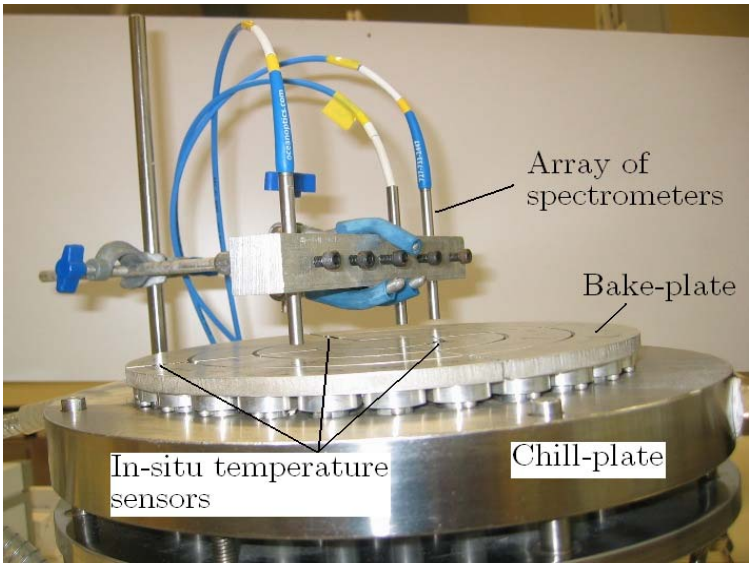

Figure 3: Integrated thermal processing system.

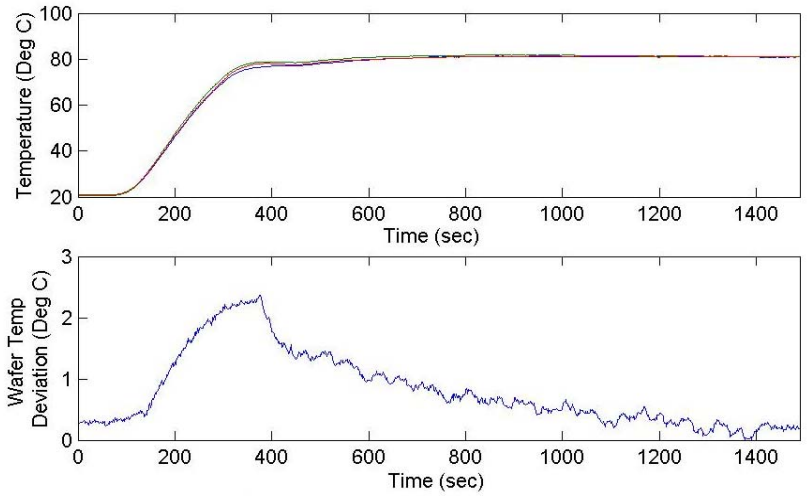

Figure 4: Temperature control of a 200 mm silicon wafer measured by 3 in-situ RTDs sensors. The lower plot shows the temperature uniformity during the entire baking process.

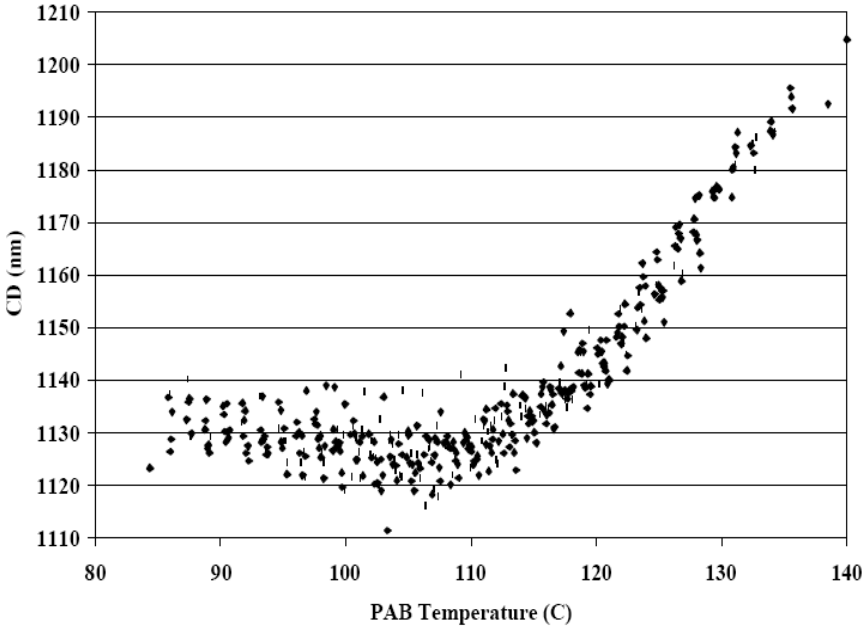

Figure 5: The sensitivity of the linewidth of a quartz photomask to post-apply bake temperature as determined from a single experimental run. The thermal array was controlled to 49 separate temperature setpoints incremented uniformly within the range of 80 to 140C. The linewidth, or critical dimension (CD), in one of the legs of a cross was mapped to the corresponding positional location of the hotplate temperature.

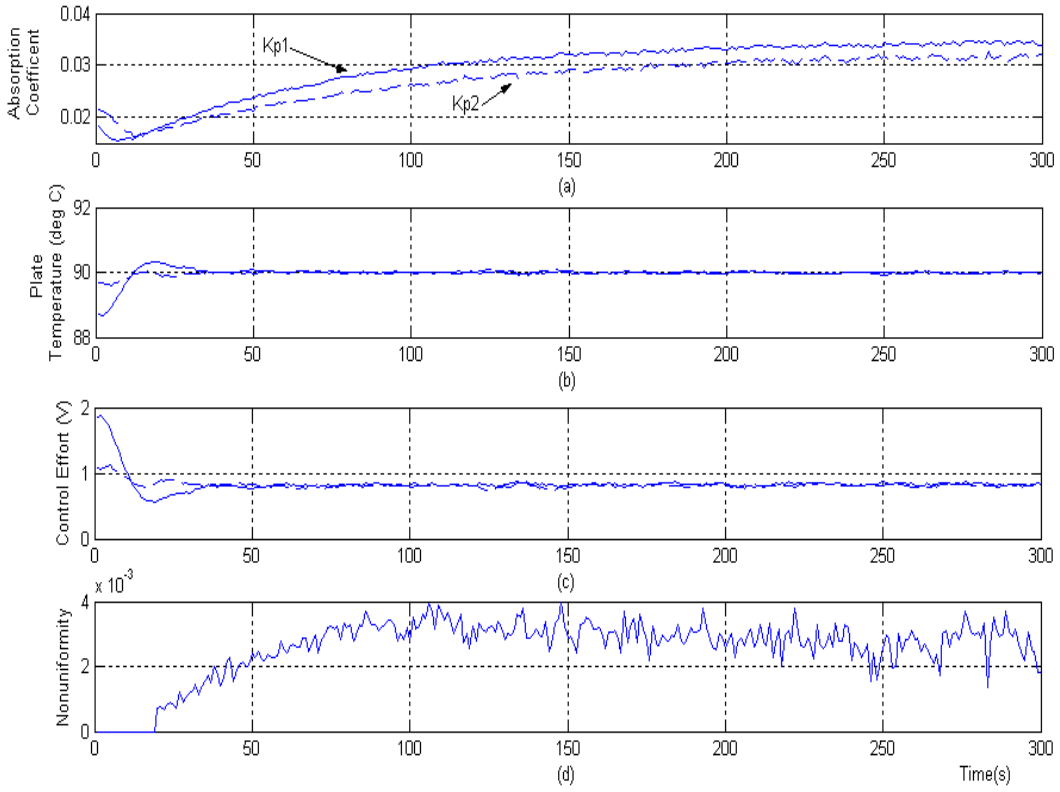

Figure 6: Conventional softbake with bakeplate maintained at 90^oC: site 1 and site 2 are represented by dashed and solid lines respectively. (a) Absorption coefficient, (b) Plate Temperature, (c) Control, (d) Absorption coefficient uniformity.

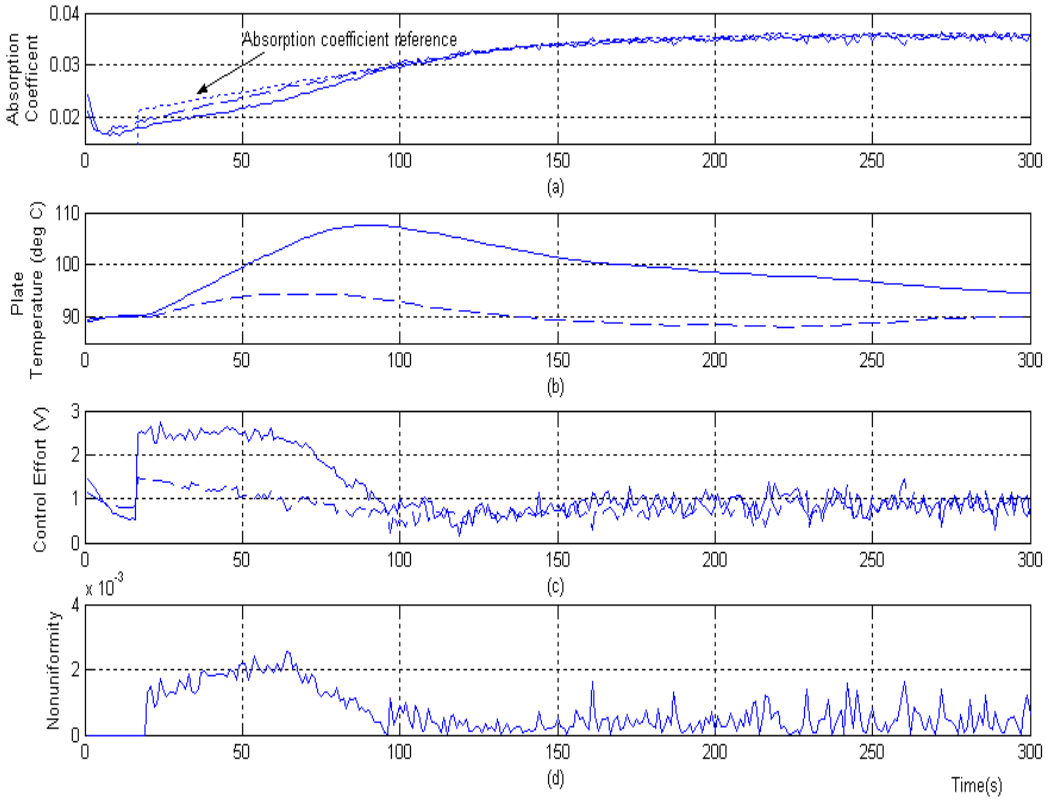

Figure 7: Softbake with multizone bakeplate: site 1 and site 2 are represented by dashed and solid lines respectively. (a) Absorption coefficient, (b) Plate Temperature, (c) Control, (d) Absorption coefficient uniformity. The reference thickness trajectory is given by the dotted line.

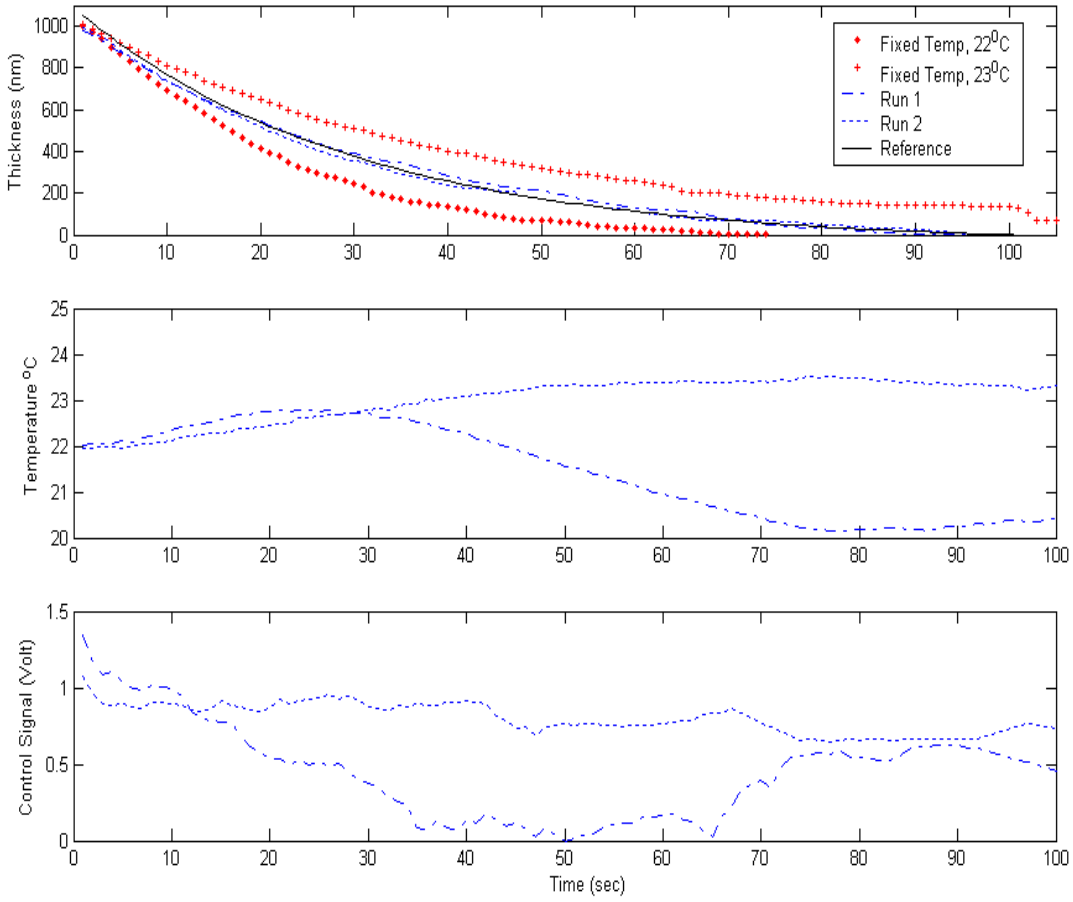

Figure 8: Photoresist development experiment. (a) Absorption coefficient, (b) Plate Temperature, (c) Control. The reference thickness trajectory is given by the solid line. Run 1 and 2 in dash-dotted and dotted line demonstrate real-time control of the development process to follow a reference trajectory. The "◇" and "+" corresponds to conventional development process with the developer at different temperature.