Deposition and characterization of ultra thin hafnium and zirconium silicate films on Si(100) using metal complexes of alkoxide and amido groups.

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Aggressive scaling has led to SiO_2 gate dielectrics less than 1.5 nm in sub 0.1 μm CMOS technologies but at these thickness a direct leakage current becomes unacceptably higher than allowed value from electron tunneling through SiO_2 ultra thin layer.[1] Hafnium or zirconium silicate [$Hf_xSi_{1-x}O_y$ or $Zr_xSi_{1-x}O_y$] films are the most promising candidates to replace SiO_2 (k=3.9) gate dielectrics in complementary metal-oxide-semiconductor (CMOS) devices. The trend of the Hf-Si-O and Zr-Si-O systems is much similar, because Hf and Zr have the ssimilar chemical properties.[2] Hf and Zr-silicate, which have three times higher dielectric constants than that of SiO_2, generally show good thermal stability and high quality interfaces in direct contact.[3]

In this work Hf- and Zr-silicate metal-organic chemical vapor deposition (MOCVD) and atomic layer chemical vapor deposition (ALCVD) were studied for high dielectrics gate oxides. The precursor combination of tetrakis-diethylamido-hafnium or zirconium [Hf or $Zr(NEt_2)_4$] and tetra-n-butyl-orthosilicate [$Si(O^nBu)_4$] was used. These deposition techniques were generally preferred for depositing ultra-thin films to ensure a highly conformal, uniform thin film growth.[3] ALCVD is a special modification of the CVD technique, based on the self-limiting surface reactions, which accurately and simply controls the film thickness and composition.[4]

As a gate oxide becomes thinner, the interfaces and uniform film have shown to play a key role in device performance. High-resolution TEM, AFM, SEM, XRD, and XPS were used to characterize physical properties of silicate films. Figure 1 (a) shows a high-resolution TEM and SAED images of ~7 nm Zr-silicate film grown on Si substrate at 400 °C. The interface of silicate/silicon was seen to be atomically sharp with no interfacial silicon oxide layer, and the silicate was completely amorphous, which was also ascertained from SAED

image. The SEM image of 65 nm Hf-silicate film shows the flat interface and uniform surface grown on Si at 400 °C [Fig. 1 (b)].

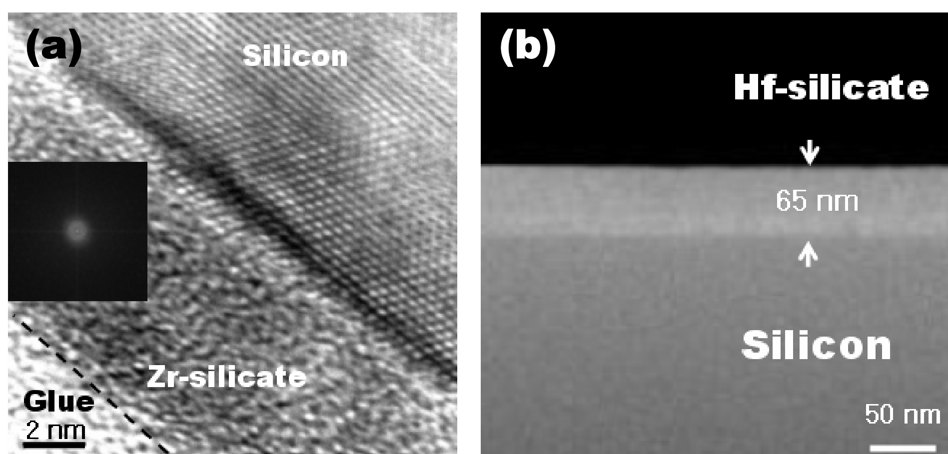

Figure 1 (a) High-resolution TEM image of an interface between a silicon substrate and a 7 nm zirconium silicate film grown by CVD. The inset shows the corresponding electron diffraction pattern of zirconium silicate parts. (b) SEM image of a 65 nm hafnium silicate film on a silicon substrate deposited by CVD.

Deposition rate was measured as a function of the substrate temperature at a constant reactor pressure of 0.1 Torr. Figure 2(a) shows the Arrhenius plot of the deposition rate of the Zr-silicate CVD using $Zr(NEt_2)_4$ and $Si(O^nBu)_4$ precursors. The apparent activation energy of ~9.5 kcal/mol was obtained. For substrate temperatures above 500 °C, it appears that the precursor was dissociated in the gas phase leading to the decrease of the deposition rate.

In order to accurate the thickness control and deposition of ultra-thin uniform films, ALCVD process was performed. In ALCVD the film thickness can be controlled by the number of reaction cycles. The dependence of growth rate on deposition temperature of Hf-silicate ALCVD using $Hf(NEt_2)_4$ and $Si(O^nBu)_4$ was investigated in the temperature region of 200-450 °C. Figure 2(b) shows that the growth rate was almost constant in 290~350 °C, which is the ALCVD window of our results. The saturated growth rate was 1.1 Å/cycle in our results, which is lower than 3~4 Å/cycle in ALCVD study using $Hf(N(CH_3)_2)_4$ and (*t*-$BuO)_3SiOH$.[5] We believe that the lower growth rate results from the difference of self-limiting nature, thermal stability, and ligand size.

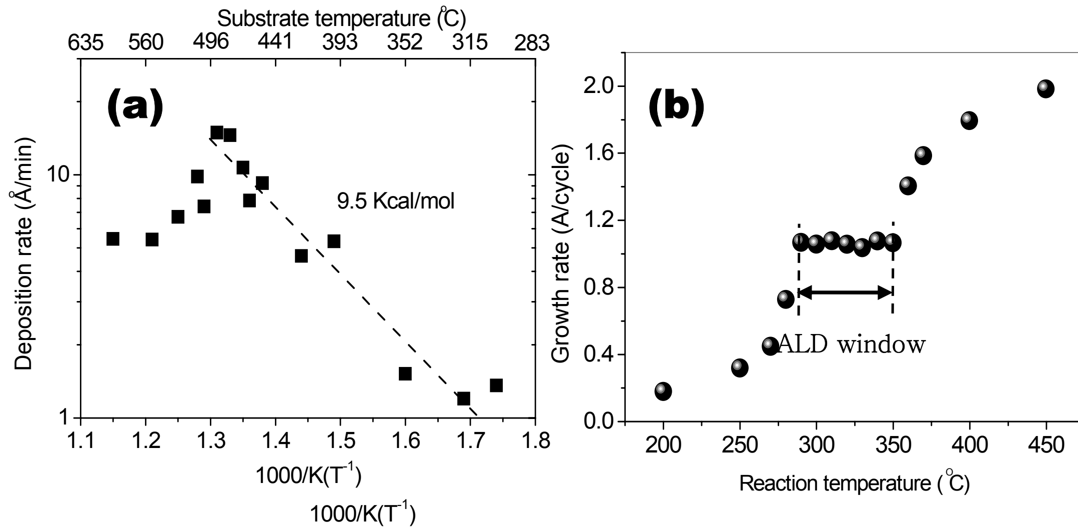

Figure 2 (a) The arrhenius plot of the deposition rate of Zr-silicate film on Si(100) grown by CVD. (b) The growth rate on Hf-silicate as a function of substrate temperature ($Si(O^nBu)_4$ pulse: 10 s, $Hf(N(C_2H_5)_2)_4$ pulse: 11 s, purge: 7 s).

Figure 3 (a) shows capacitance-voltage (*C-V*) results, flatband voltage (V_{fb}) and the electrical equivalent thickness (t_{eq}) obtained from ~18 nm $Hf_{14}Si_{24}O_{62}$ films. Capacitors were fabricated using gold (Au) *ex-situ* thermal evaporation. Area of gold gate electrode was 5.11×10^{-4} cm^2. We deposited the ~18 nm $Hf_{14}Si_{24}O_{62}$ film at 300 °C and annealed it using RTA method at 600 °C, 700 °C, and 800 °C in N_2 atmosphere for 15 s to improve the film quality. The maximum capacitances of as-deposited, 600 °C, 700 °C, and 800 °C annealed films were 247, 259, 290, and 274 pF, respectively. These results correspond to k values of 9.7, 10.3, 11.5, and 10.9, respectively. The capacitance of Au/Hf-silicate/Si structures was increased upto 700 °C and reversely decreased at 800 °C. Above 800 °C we believe that the interfacial layer is increased, which results in the decrease of capacitance. The slopes of *C-V* curves of the N_2 RTA films near by center were very steep, indicating a low density of interface states, while that of the as-deposited film was slightly stretched compared to one measured after annealing.[6] The flat band voltages were positively shifted from -1.76 V (as-deposited film) to -0.14 V (800 °C), because the effective positive charge by oxygen vacancies decreased with annealing.[7] Hysteresis was also lowered from 0.88 V (as-deposited) to 0.19 V (800 °C RTA), because the trapped charges at defect sites were reduced.[8]

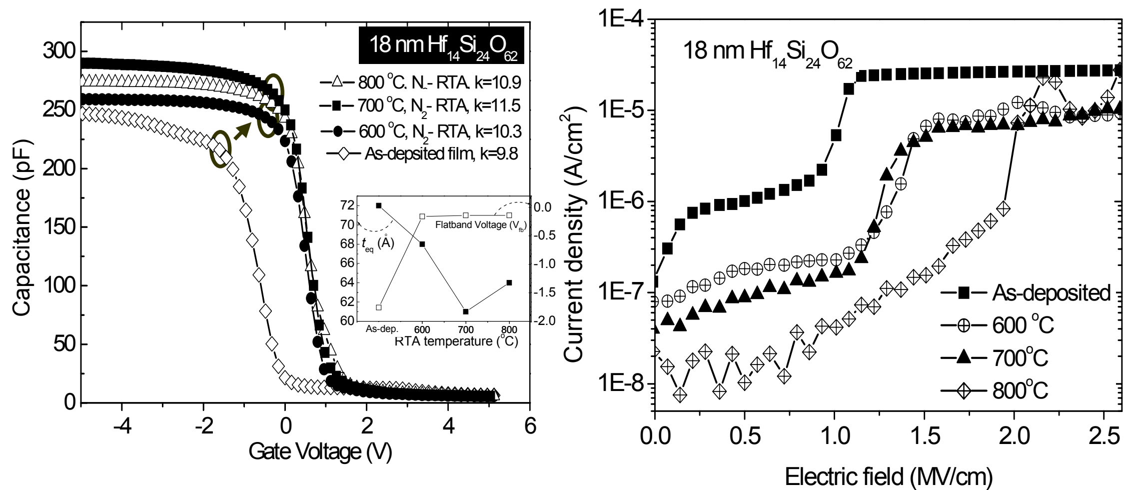

Figure 3 (a) High-frequency (1 MHz) *C-V* curves, t_{eq}, and flat band voltage (V_{fb}) of thin hafnium silicate films as a function of annealing temperature (°C) for a silicate film with the Hf/(Hf+Si) of 0.37. The figure 3 (b) shows the corresponding *I-V* curve as a function of annealing temperature (°C), in which the leakage current density was decreased from 9.2×10^{-6} A/cm^2 (as-deposited) to 6.8×10^{-8} A/cm^2 (800 °C RTA) at a bias of 1 MV/cm.

The current-voltage (*I-V*) characteristics for the same ~18 nm $Hf_{14}Si_{24}O_{62}$ film as a function of electric field (MV/cm) are shown in the figure 3(b). The leakage current density was reduced from 9.2×10^{-6} A/cm^2 (as-deposited) to 1.6×10^{-7} A/cm^2 (700 °C RTA) at a bias of 1 MV/cm.

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