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Modeling and Synthesis of DES Supervisory Control for Coordinating ULTC and SVC

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***Abstract*— Discrete-event systems (DESs) can be found as an essential integrated subsystems in electrical power systems. The supervisory control theory is a general theory for synthesis of controllers for DESs. Under-load tap-changing transformers (ULTC) which obviously have discrete-event behavior are widely used in transmission systems to take care of instantaneous variations in the load conditions in substations. Also, the static VAR compensator (SVC) which has fast dynamic characteristic can be used to support system voltage following disturbance. The combination of an SVC and a ULTC can not work properly on the same bus without appropriate coordinated control rules as these two devices are designed to achieve voltage regulation target based on their own measurements. The paper discusses the issues involved in modeling and synthesizing of a supervisory control system in centralized and decentralized structures to coordinate the behavior of the ULTC and the SVC. The control specifications are modeled as some automata and it is shown that they are controllable. The designed closed loop control system is non-blocking.**

I. INTRODUCTION

Power systems exhibit interactions between continuous dynamics and discrete events frequently. The power system, in its simplest representation, comprises of a set of lines intersecting at nodes (buses). Under-load tap-changing transformers are the most widely used voltage regulation device in power networks. They can be found on nearly all the transformers operating at 13.8kV or above [1]. ULTC is not capable of providing fast response to changes for voltage sensitive load. On the other hand, Static VAR Compensator (SVC) is an extremely fast voltage regulation device, but its regulation ability is restricted by its rating. Therefore, where ULTC and SVC are installed on the same load supply bus for voltage regulation purpose, the drawbacks of one can be compensated by the other. However the combination of these two devices can not work properly on the same bus without appropriate coordinated control rules because they are designed to achieve voltage regulation target based on their own measurements.

The coordination of ULTC with a VAR compensator such as STATCON, STATCOM or SVC has been studied in several research works [2-6]. A SVC control strategy with two stages of regulation slopes and two voltage regulation controls was proposed by [6] to coordinate SVC with ULTC; however, the impact of the SVC operation condition on the ULTC behavior was not considered.

All the attempts apparently showed the necessity for coordination of ULTC with VAR compensator equipments such as an SVC. Indeed, when both SVC and ULTC are used to control the system voltage, the SVC reacts to the voltage deviation faster than ULTC. If SVC output reaches the maximum capacity limit, it loses active control and behaves similar to a shunt capacitor bank. The SVC output may reach its maximum output due to the steady-state load increase or system disturbance. Therefore, for optimum usage of the installed equipments (ULTC & SVC) in an electrical power network, a coordinated control system should be utilized.

Because of the event-based nature of ULTC and the switching behavior of SVC control strategy, the overall system has been modeled as a discrete-event system (DES) in this paper. The supervisory control (SC) theory is a general theory for synthesis of controllers for DES. A discrete-event system is a dynamic system that evolves in accordance with the sudden occurrence of physical events at possibly unknown irregular intervals [7]. Applications of DES theory to power systems [8-13] include: (i) supervisory control, (ii) modeling and analysis, (iii) monitoring and diagnosis, and (iv) physical implementation problems. We used DES Supervisory Control theory to synthesize a controller which coordinates the behavior of the ULTC and SVC. The main advantages of this approach can be summarized as follows:

1- Although, components of a ULTC control system are simple devices, its overall behavior is complex due to time delays, dead band, and etc. This behavior can be easily considered in Supervisory Control theory.
2- The SVC control strategy has a hybrid nature that involves both the continuous and discrete dynamics. The control of such a complex system in the hybrid framework is very difficult. Here, we propose an approach in which the continuous dynamics of the SVC have been controlled by a traditional controller, e.g. a PI controller, and the switching behavior of SVC have been supervised by a DES supervisory control.

To the author's knowledge the control strategies for the ULTC and SVC, which are used in this paper, have not considered concurrently before. Also, DES modeling and synthesis of supervisory controller for SVC and ULTC coordination has not been addressed before and is introduced in this paper for the first time

Section 2 briefly reviews the DES supervisory control. The proposed coordination between ULTC and SVC is presented in section 3. The DES modeling of the plant as

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well as the control logic, and the design and implementation of the supervisory control using DES in centralized and decentralized structures are discussed in section 4. Finally, we make the conclusions in Section 5.

II. DES Supervisory Control Theory

The supervisory control problem for a discrete-event system is formulated by modeling the plant as well as its control logic (specifications) as some DES. To solve the supervisory control problem, it is necessary to show that a controller which forces the specification to be met exists and is constructible. DES supervisory control is briefly described in this section; the reader is referred to [14] for more details.

A DES model is specified by; the set of states (including an initial state, and marker state which can be desired states in some applications), the set of events, and the state transition function of the system. Formally, a DES is represented by an automaton G = (Q, Σ, δ, q_0, Q_m) in which; Q is a finite set of states, with $q_0 \in Q$ as the initial state and $Q_m \subseteq Q$ being the desired (marker) states; Σ is a finite set of events (σ) which is referred to as an alphabet; and finally δ(q, σ) is a transition mapping δ: Q×Σ →Q which gives the next state after occurrence of an event (σ). G plays the role of the plant and together with its states, events and transition operator (mapping) model a physical process. G is called generator, as it generates a set of strings (sequence of events or concatenated events). In other words it generates a language L(G), consisting of strings of events which are physically possible in the plant.

The supervisor controls the behavior of a discrete-event system by enabling and disabling events, therefore affects the event sequences and state trajectories of the plant. The supervisor can be considered as a function $V : L(G) \to \Gamma$. $\Gamma(\sigma) = 0$ means that the event σ is disabled and $\Gamma(\sigma) = 1$ indicates that the event σ left enabled. It is often possible to meet these specifications in a minimal restrictive way which is addressed by optimal supervisor in DES literature [14]. As an alternative method, one may design a modular supervisor for each control specification in a similar way. The decentralized supervisors are valid provided the resulting controlled behaviors are not conflicting.

TCT software program is developed for modeling and synthesis supervisory control for discrete-event systems in different structure. There are other software tools available for simulation and analysis of DES [15].

III. ULTC and SVC Coordination Control

Transformers with tap-changing facilities constitute an important means of controlling voltage throughout electrical power systems in all voltage levels. Transformers with ULTC are widely used in transmission systems.

Nowadays, SVC is one of the key elements in power systems to improve power quality and reliability because of its fast response. SVC has the functional capability to handle dynamic conditions, such as transient stability and power oscillation damping in addition to providing voltage regulation [1].

ULTC is not capable of providing fast response to changes for voltage sensitive load. On the other hand, SVC is an extremely fast voltage regulation device, but its regulation ability is restricted by its rating. Therefore, where ULTC and SVC are installed on the same load supply bus for voltage regulation purpose, the drawbacks of one can be compensated by the other. However the combination of these two devices cannot work properly on the same bus without appropriate coordinated control rules because they are designed to achieve voltage regulation target based on their own measurements.

A. *Modifications in ULTC control system to be Coordinated with SVC*

In order to reserve the operating margin of SVC, the time delay of ULTC can be changed adaptively, according to the operating condition of SVC. The information of SVC transferred to ULTC includes the value and changing direction of the SVC susceptance. The adaptive adjustment process relieves the load of SVC through transferring its duty to ULTC. The time delay of the ULTC is determined based on the proposed algorithm in Fig 1. As shown in this figure, when the compensation current of the SVC is increasing beyond some predefined values, the ULTC operation speeds up in three levels. If an event in the electrical network causes a decreasing in the SVC capacity, the ULTC is delayed as much as possible.

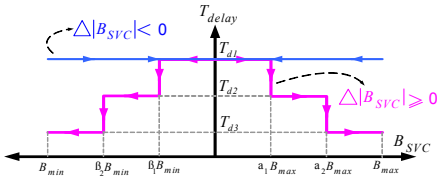

Fig. 1. Proposed algorithm for adjustment of the timer of ULTC based on SVC susceptance

B. *Modifications in SVC control system to be Coordinated with ULTC*

SVC characteristic can be used to limit the reactive power output from SVC to a desired value during the steady-state voltage range and also to compensate the reactive power requirement from the upstream networks via the coordination with ULTC [6]. The V-I characteristic of SVC is shown in Fig. 2. The fixed-voltage reference control is used to regulate the voltage within steady-state margins. When the controlled voltage crosses out the switching points (steady-state voltage range), the floating-voltage reference control is utilized to rapidly regulate the voltage and slowly return the SVC output back to the steady-state margin. The switching logic between the fixed-voltage reference control with regulation slope X_{SL1} and the floating-voltage reference control with the regulation slope X_{SL2} is summarized as follows.

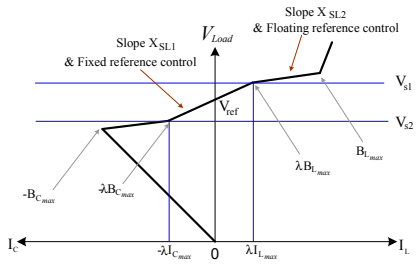

Fig.2. V-I characteristics of the SVC

1) When the controlled-bus voltage is within the desired SVC switching points, the fixed-voltage reference control with the slope X_{SL1} is switched on.

2) When the controlled-bus voltage crosses out the desired switching points, the floating-voltage reference control with the slope X_{SL2} is switched on.

3) The changeover from the floating-voltage reference control to a fixed-voltage reference control is utilized when the SVC output is returned back to the steady-state margin.

IV. Supervisory Control Synthesis for Coordination of the ULTC and SVC

Fig. 3 shows the block diagram of the supervisory control system, which coordinates ULTC and SVC behaviors. To synthesize the supervisory control, DES models of the plant and the governing control logic should be developed.

A. Discrete Event Modeling of the Plant

DES model of the plant can be synchronized by combining the models of its components namely ULTC and SVC.

1) DES Modeling of ULTC

Fig. 4 shows the block diagram of the control system for changing the transformer taps, considering the SVC interaction. It can be seen that the control system consists of four components: Voltmeter, Timer, Tap-changer, and Timer adjustment unit. Each component is modeled as a DES. Moreover, we need a model for the "operator action" to switch the operation modes (Auto/Manual) and to override in abnormal situations. DES models of the plant components are synchronized to form the plant model.

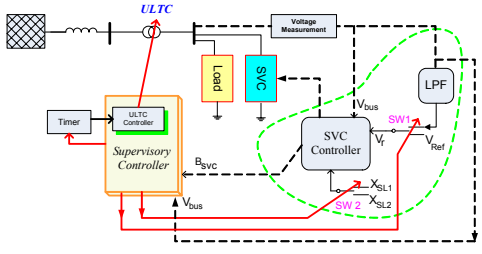

Fig. 3. Block diagram of the Supervisory control system

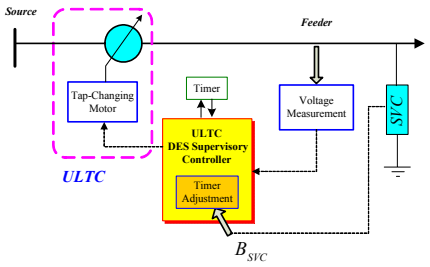

Fig. 4. Block diagram of the control system for changing transformer taps.

TIMER

The timer times out after a certain delay *Operating Time*. Following events are associated with the timer (Fig. 5.a):

Timer starts	(ev21)
Timer Blocks and Resets	(ev25)
Timer Times out	(ev28)
Timer Resets	(ev23)

TAP-CHANGER

The tap changer controls the transformer ratio "manually" or "automatically" in order to keep the power supply voltage practically constant, independently of the load. If the tap increase (decrease) is successful, the system returns to a state and waits for another command. If the tap increases (decreases) operation fails, the controller changes to Manual mode, and waits for another command.

It is assumed that the tap-changer has 5 steps. Events associated with the TAP-CHANGER are (Fig. 5.b):

Tap down command	(ev31)
Tap down successful	(ev32)
Tap up command	(ev33)
Tap up successful	(ev34)
Tap up/down failed	(ev30)

VOLTMETER:

The load voltage must be within a dead-band. Voltmeter reports following events associated with the load voltage: (Fig. 5.c):

Voltmeter Initialized	(ev11)
Report $\|\Delta V\| >$ ID and ΔV is Negative	(ev10)
Report $\|\Delta V\| <$ ID (Voltage Recovered)	(ev12)
Report $\|\Delta V\| >$ ID and ΔV is Positive	(ev14)
Report Voltage exceeds V_{max}	(ev16)

TIMER ADJUSTMENT UNIT

The Timer-Adjustment unit receives information from the SVC and sends information to adaptively adjust the ULTC time delay.

Following events are associated with the timer-adjustment block (Fig. 5. d):

$(0 \le B_{svc} \le \alpha_1 B_{\max})$ or $(\beta_1 B_{\min} \le B_{svc} < 0)$	(ev60)
Delay Time sets to T_{d1}	(ev61)
$(\alpha_1 B_{\max} < B_{svc} \le \alpha_2 B_{\max})$ or $(\beta_2 B_{\min} \le B_{svc} < \beta_1 B_{\min})$	(ev62)
Delay Time sets to T_{d2}	(ev63)
$(\alpha_2 B_{\max} < B_{svc} \le B_{\max})$ or $(B_{\min} \le B_{svc} < \beta_2 B_{\min})$	(ev64)
Delay Time sets to T_{d3}	(ev65)
$\Delta\|B_{svc}\| < 0$	(ev66)
Delay Time sets to $T_{switching}$	(ev67)
SVC susceptance measurement unit initialized	(ev69)

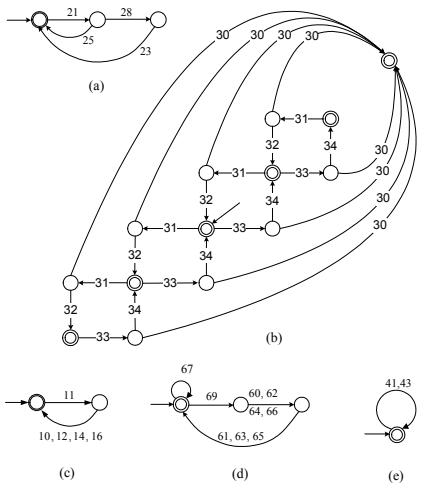

Fig. 5. DES models for (a) Timer, (b) Tap-Changer, (c) Voltmeter, (d) Timer-Adjustment, and (e) Operator

OPERATOR:

Operator can switch operation mode of ULTC using the following Events (Fig. 5. e):

Enter "Automatic" Mode	(ev41)
Enter "Manual" Mode	(ev43)

2) SVC Discrete Event Modeling

Considering new SVC V-I characteristic which was reported recently in [6], it is clear that SVC control system has hybrid dynamics behavior including both continuous and discrete dynamics. Since the control of such a complex hybrid system is difficult, we propose an approach in which the continuous dynamic of SVC is controlled by a traditional PI controller, while the switched behavior of the SVC is supervised by a DES supervisory control system. The block diagram of the proposed SVC control system is shown in Fig. 6. The PI controller and the DES supervisor operate concurrently. The hybrid (combined) controllers implement the SVC characteristic, shown in Fig. 2.

For the purpose of the SVC modeling in a DES framework, it is enough to consider only the discrete-event behavior of SVC. As shown in Fig. 6, the SVC supervisor receives the bus voltage and SVC susceptance information and adjusts the feedback gain and the set point of the control loop using these measurements. Therefore, the overall discrete-event behavior of the SVC can be stated by combining the following three models: Voltmeter, Susceptance Meter, and a switch which adjusts the required parameters. These DES models are shown in Fig. 7.

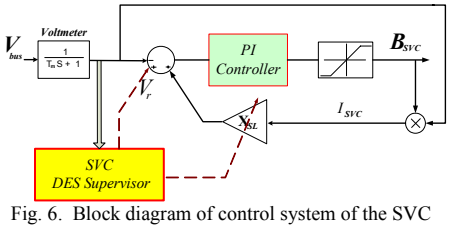

Fig. 6. Block diagram of control system of the SVC

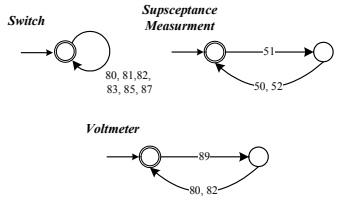

Fig. 7. DES models for the SVC control system components

Following events are associated with the SVC DES model (Fig. 7.):

Susceptance measurement initialized	(ev51)
$-\lambda B_{C\max} \le B_{svc} \le \lambda B_{L\max}$	(ev50)
$B_{svc} < -\lambda B_{C\max}$ or $B_{svc} > \lambda B_{L\max}$	(ev52)
$V_{S2} \le V_{load} \le V_{S1}$	(ev80)
Fixed-voltage reference control is switched on	(ev81)
$V_{load} > V_{S2}$ or $V_{load} < V_{S1}$	(ev82)
Floating-voltage reference control is switched on	(ev83)
The regulation slope X_{SL1} is switched on.	(ev85)
The regulation slope X_{SL2} is switched on.	(ev87)
Voltmeter Initialized	(ev89)

B. DES modeling of the Control Logic

A discrete-event plant must be controlled based on some specifications (requirement behavior). In this section the control logic of the ULTC and SVC are presented in details and are modeled as some DES.

1) ULTC Control Logic

The control logic for tap-changer transformers can be found in the literature [16] as well as in manufacturers' catalogues (e.g. [17]) in different details. The ULTC control logic can be summarized as follows: When the voltage is not "normal", then the controller changes tap ratio after a time delay to restore the voltage i.e. bring it back into its dead-band. The delay time, which is determined based on the SVC operation condition in this paper, is used to prevent unnecessary tap changes in response to transient voltage variations. So the tap-changer works in Auto/Manual mode according to the following logic (control specifications):

a. If the voltage deviation $|\Delta V| >$ ID and ΔV is Negative (ev10) then the timer will start and when it "times out" i.e. reaches its maximum (e27) then a "tap increase command" (ev33) will be made and the timer will be "reset" (ev23).

b. If the voltage deviation $|\Delta V|>$ID and ΔV is Positive (ev14) then the timer will start and when it "times out" (e28) then a "tap decrease command" (ev31) will be made and the timer will be "reset" (ev23).

c. If the voltage returns to the dead-band (ev12), because of smooth system dynamics or a tap change or some other system events, then the timer is blocked and reset (ev25).

d. If the voltage exceeds the value set for "Quick Lowering" (ev16), then the timer becomes 0 seconds

and therefore the lowering tap command (ev31) happens instantaneously.

e. If a fault in tap increase or decrease happens (ev30), or operator forces the system from Automatic to Manual mode at any time (ev43) the system moves to the manual state and waits for the operator.

f. The time delay of the ULTC is determined based on the SVC operation condition as shown in Fig. 1. When the applied susceptance of the SVC is increasing, the time delay of the ULTC will be decreased stepwise. On the other hand, when the applied susceptance of the SVC is decreasing, the time delay of the ULTC is set to its maximum value.

g. After of a tap movement, if another tap changing is required in the same direction, the time delay is set to $T_{switching}$ (minimum possible value for the time delay).

The above logic is implemented by two DES models which are shown in Fig. 8. "Manual" command (ev43) takes the system from any state (*) to the Manual-operation state. Then ev41 takes this state back to the initial state. Also, if a fault in tap increase or decrease happens (ev30), the system moves to the manual state and waits for the operator actions.

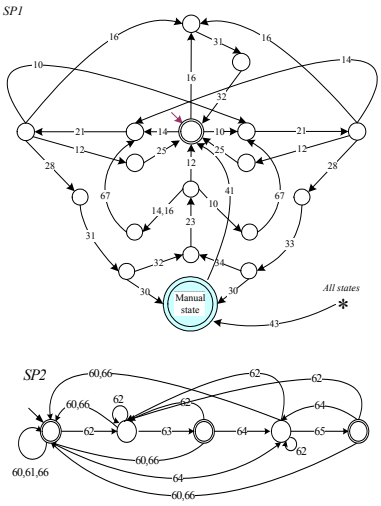

Fig. 8. DES models for ULTC control specifications (Sp1 and Sp2) in the Auto/Manual mode.

2) SVC Control Logic

The SVC has a hybrid nature. As shown in Fig. 6, its continuous dynamic is controlled by a PI controller. The SVC supervisor is responsible to supervise the SVC discrete-event dynamic based on some control specifications that have been extracted form SVC V-I characteristic as follow:

a. When the controlled-bus voltage is within the desired SVC switching points (ev80), the fixed-voltage reference control with the slope X_{SL1} is switched on (ev81 & ev85).

b. When the controlled-bus voltage crosses out the desired switching points (ev82), the floating-voltage reference control with the slope X_{SL2} is switched on (ev83 & ev87).

c. When the SVC output is returned back to the steady-state margin (ev50), the changeover from the floating-voltage reference control and slope X_{SL2} to a fixed-voltage reference control and slope X_{SL1} is utilized. (ev81 & ev85).

Fig. 9 shows the DES model of the SVC control specifications. It actually implements all above logics in a single DES.

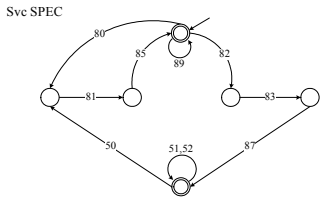

Fig. 9. DES models for SVC control specification

C. Supervisory Controller Synthesis

Using the specification and the plant model the supervisory control can be synthesized using TCT software program which is developed for modeling and synthesis supervisory control for discrete-event systems [14].

Based on the proposed DES models for the plant and the control specifications of the ULTC and the SVC, a supervisory control is synthesized as a coordinator. In the following sections the systematic synthesizes of the supervisory control system in centralized structure as well as the decentralized structure are discussed.

1) Centralized structure

Firstly, the DES model of the plant is computed by synchronizing the ULTC model and SVC model:

PLANT = Sync(ULTC-PLANT, SVC-PLANT) (1008,15896)

The second stage is to combine all specifications:

Specification= Meet(ULTC_SPEC,SVC_SPEC) (1230,12778)

Then the supervisory control, which coordinates the behavior of ULTC and SVC based on the predefined specifications, is computed:

Supervisor = Supcon(PLANT, Specification) (10800,53532)

M-Supervisor= Minstate(Supervisor) (3728,18788)

The size of a DES model is given by the number of states and number of transitions. The size of the supervisor is, (10800, 53532). After applying the ''Minstate'' operation the supervisor state-transition size is reduced (3728, 18788) which still is a large automaton for implementation porpouse. ''Minstate'' reduces the supervisor to a minimal state transition structure that generates the same closed and marked languages.

2) Decentralized structure

One of the basic problems in the SC framework is related to the real-time implementation of a supervisor [13]. The

most important problem in the implementation stage is the size of the supervisor. Here, because of the large size of the designed centralized supervisor, we should look for other structures such as decentralized structure which provides the supervisory control with a smaller automaton in size for easier implementation. In the decentralized structure, we design the modular supervisory control using the specifications, which are defined for ULTC and SVC, separately. Each supervisor controls one part of the plant.

ULTC_Supervisor = Supcon(ULTC, SP12) (1350,5004)
M-ULTC_Supervisor=Minstate(ULTC_Supervisor) (466,1766)
SVC_Supervisor = Supcon(SVC-PLANT,SVC-SPEC) (8,10)

The modular supervisor for SVC is shown in Fig. 10. Since the size of the ULTC supervisor still is large (1350,5004), we use the decentralized structure again to synthesis the ULTC supervisory control system in a modular framework. Each of the control specifications of the ULTC (Fig. 8) is implemented by one modular supervisor:

ULTC_SUP1 = Supcon(LOCAL-PLANT1,SP1) (267,1067)
ULTC_RSUP1 = Supreduce(L-PLANT1,SP1, Control-Data1) (15,73;slb=15)
ULTC-SUP2 = Supcon(LOCAL-PLANT2,SP2) (9,18)

Three supervisors namely SVC_supervisor, ULTC_Sup1, and ULTC_Sup2 implement the overall supervisory control system which coordinates ULTC and SVC. These supervisors operate concurrently, that possible conflict with each other and with the plant should be checked.

It can be seen that they operate concurrently without any possible conflicting or Blocking:

true = Nonconflict(ULTC_Sup1,ULTC_Sup2)
true = Nonconflict(ULTC_Sup1,SVC_Supervisor)
true = Nonconflict(ULTC_Sup2,SVC_Supervisor)
true= Nonconflict(ULTC_Sup1&2,SVC_Supervisor, PLANT)

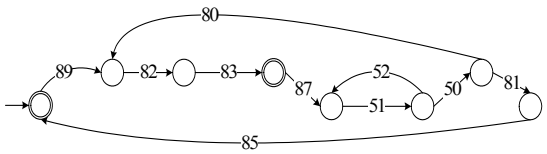

Fig. 10. Automaon of SVC_Supervisor

V. CONCLUSION

Under-load tap-changing transformers are the most widely used voltage regulation devices in power networks, but they are not capable of providing fast response for voltage sensitive load. On the other hand, Static VAR Compensator is an extremely fast voltage regulation device, but its regulation ability is restricted by its rating. It has been completely discussed that for the optimum usage of the potential of the installed equipments (ULTC & SVC) in an electrical power network, a coordinated control system.

A Non-blocking supervisory control to coordinate the SVC and the ULTC was synthesized. The ULTC and the SVC components and their control specifications have been modeled as some automata. Controllability of the specification is evaluated and supervisory controllers have been designed in centralized and decentralized structures using TCT software program. It is guaranteed by the synthesis procedure that the designed supervisors are optimal and non-blocking. The state size of the supervisory controller has been reduced for easier implementation purposes. The decentralized structure simplifies the implementation of the proposed supervisory control on a programmable logic controller.

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