Real Time Digital Simulations Augmenting the Development of Functional Reconfiguration of PEBB and Universal Controller

W. Ren, L. Qian, Y. Liu, M. Steurer, D. Cartes

***Abstract* —In this paper, real-time hardware-in-the-loop (HIL) simulation is adopted to augment the development of functional reconfiguration of power electronic building blocks and universal controllers. The simulation environment employs a commercial real-time digital simulator allowing real time simulations of large power systems. Two case studies regarding functional reconfiguration are discussed. The first case is a marine all-electric-ship application to improve system power quality. A novel control algorithm is proposed for an active filter, which is derived from reconfiguring variable speed motor drive. The second case outlines how the HIL simulator is utilized to a static synchronous compensator application where a commercial controller provides firing pulses to a simulated converter and the connected power system. Details of the control scheme, the HIL setup, and test results are given.**

***Index Terms*—power electronics, control, real-time simulation, hardware-in-the-loop simulation, all-electric ship.**

NOMENCLATURE

C	capacitance of the DC link capacitor
C_f	capacitance of the filter capacitor
I	line current coming out of the bridge
I'	line current coming into the grid
L	total inductance of the line reactors
U	grid side voltage
U_{dc}	DC voltage across the DC link capacitor
V	bridge side voltage
ω	rotation speed in rad/sec
d	switching functions
d,q	subscript for d and q axis value respectively
ref	subscript for reference or command value

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W. Ren, L. Qian, Y. Liu, M. Steurer, and D. Cartes are with the Center for Advanced Power Systems at Florida State University, Tallahassee, FL, 32310, USA (Internet: http://www.caps.fsu.edu, e-mail: rren@caps.fsu.edu, qien@caps.fsu.edu, steurer@caps.fsu.edu, yliu@caps.fsu.edu, dave@eng.fsu.edu, and phone (D. Cartes): 850-645-1184; fax: 850-644-7456)

I. INTRODUCTION

With the rapid development of solid-state technology, power electronic devices are being extensively used in electrical power systems, aerospace, naval ships, and industries. A key issue of applying power electronic devices in different industries is the reduction of cost, losses, size, and weight of power electronics [1]. Power electronic building blocks (PEBBs), first proposed by Ericsen [2], are used to reduce the cost, manning, and maintenance of power electronic devices installed in military marine applications. Later, industry adopted the idea for civil applications [3]. PEBBs are generally composed of many sets of semiconductor devices, or phase legs, or functional subsystem blocks. They can be easily reconfigured, both in hardware and software, to realize different functionalities. A universal controller (UC) is a multi-function controller board designed to provide control algorithms to PEBB and adjust their configurations.

Beyond the reduction of the total cost, the combination of PEBB and UC has the advantage of easy reconfiguration. The latter can be classified into static reconfiguration (e.g. change of control algorithm), and dynamic reconfiguration (e.g. change of hardware topology) [2].

The traditional method to test PEBB/UC architectures is to build a scale-down power electronic (converter) system which is controlled by the UC. To decrease the cost and time of development and test real-time (RT) hardware-in-the-loop (HIL) simulation can be used. HIL is the concept of simultaneous use of simulation and real equipment. For mechanical and hydraulic systems the HIL has already become a standard research, prototyping, and testing technology in the aerospace [4] and the automobile industry [5]. First introduced for power systems to test protection relays and later HVDC (i.e., High Voltage Direct Current Transmission) control systems RT-HIL is increasingly applied in electric power R&D not only to test automatic generator synchronizers [6] and to diagnose electric machinery [7] but quite recently to effectively study power quality [8].

In this paper, RT-HIL simulation is adopted to validating the functional reconfiguration of PEBB and UC, in particular, their NAVY applications. In section II, basics of the PEBB and UC concepts are reviewed. In section III, the topology of the RT-HIL simulator installed at the Center for

Advanced Power Systems (CAPS) at Florida State University, Tallahassee, is described. Finally, in sections IV and V two case studies are presented.

II. Basis of Power Electronics Building Blocks and Universal Controller

A. PEBB

The PEBB program was originally driven by the need of the U.S. Navy to achieve lower purchase cost and life-cycle costs (such as: manning, maintenance, and fuel) [2]. PEBB has the potential of being used in a wider variety of applications in industry (e.g., HVDC, Flexible AC Transmission Systems FACTS, distributed generation, and energy storage) with a power range from hundreds of kW to thousands of MW [1].

The basic idea of the PEBB is to incorporate and standardize the integration of a set of power devices, gate drives, and other components to functional blocks for multiple applications. Fig.1 shows a pictorial of an IGBT (i.e., insulated Gate Bipolar Transistor)-based PEBB composed of a number of power electronic phase legs, energy storage device (e.g., DC capacitor C_{dc}), and communication ports (e.g., firing pulse input, reference voltage and/or current input, dc voltage and/or current output). The PEBB as shown in Fig. 1 can be configured as either a DC/AC inverter/rectifier or a DC/DC chopper (phase ABC terminals against one DC pole). Two such PEBBs connected back-to-back can be used as an AC/AC converter (e.g., variable frequency motor drives).

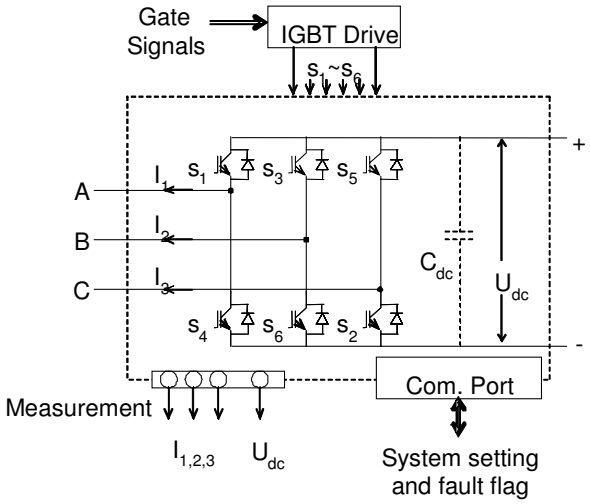


Fig. 1. Pictorial of an IGBT-based PEBB

B. Universal controller

A universal controller (UC) is a multi-function controller designed especially for the control of PEBBs. The controller provides appropriate control logic and transforms a PEBB from one application to another. Fig. 2 shows the topology of a typical UC. Generally, a universal controller consists of a high-speed CPU for program running and data processing, a number of high speed D/A converters and A/D adaptors, memory units (e.g., external flash memories, and Field Programmable Gate Arrays - FPGAs). The external flash memory is needed only when there is a need for the high volume storage in special tasks. FPGAs are used for fast logic and computational functions, and a set of software packages for program editing and compilation functions.

In this paper newly developed commercial off-the-shelf power electronic controller (AC 800-PEC from ABB) serves as the universal controller platform. The AC 800-PEC applies Matlab® /Simulink® Real Time Workshop® as the upper controller. Ethernet is used to communicate between the processor and upper controller. In the FPGA, certain functions such as PWM firing pulse generation, fault detection and handling are pre-stored and executed. Ultimately, the AC 800-PEC will be connected to an IGBT-based PEBB product ("PowerPak3") to form a complete system [9], [10].

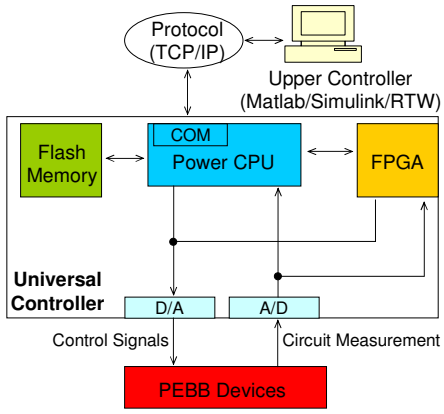


Fig. 2. Topology of a typical universal controller

C. Reconfiguration of PEBB/UC architecture

A significant advantage of PEBB/UC architecture is their capability for functional reconfiguration. Fig. 3 shows a typical schematic of PEBB/UC in a distribution system. As an inductive load motor 3 will result in a poor power factor. The diode rectifier of the drive of motor 2 will generate odd harmonic currents. If a PEBB/UC architecture is used for the variable frequency drive of motor 1, its front end rectifier can be reconfigured to either serve as an active filter to cancel harmonics, or as a STATCOM to improve the overall power factor. The functional reconfiguration is easily accomplished by implementing different control algorithms in the UC. Only changes in the passive filter components may be required. The two cases are discussed later in this paper. Both of them start from a description of the control algorithm. Computer simulations are then performed to validate the result.

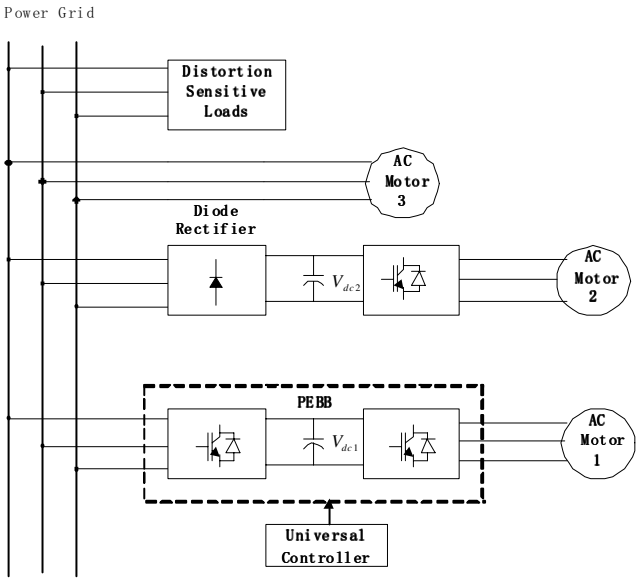


Fig. 3. Functional reconfiguration of PEBB/UC

III. Real-Time Hardware-In-The-Loop Simulation

Building an advanced RT-HIL simulation capability at CAPS has been driven by the need for research on all-electric Navy ship power systems. The platform is composed of a commercial real-time (RT) digital simulator RTDS® [11], any hardware under test, and its interface to the simulator (e.g., power amplifiers and/or signal transducers). The digital simulator can be used either as an independent simulation system (i.e., no hardware in the loop) to run in real time or non real time (but still many times faster than typical PC based simulators), or with hardware under test (necessarily in real-time).

A RT-HIL simulation experiment is set up as illustrated in Fig. 4. The tested PEBB and the distribution system are modeled in RTDS®. Simulated quantities such as nodal voltages and branch currents are transmitted through D/A converters to the universal controller. The latter receives these signals and processes them according to the control logic which has been downloaded from the Simulink / RTW. The UC feeds appropriate firing pulses back to the RTDS through time-stamped digital input (DITS) cards.

The RTDS® was initially designed for the simulation of large-scale power systems where only thyristor controlled power electronic devices are used. Hence a typical simulation time step of a reasonably complex system is around 50 μs. A proprietary advanced computation algorithm for PWM type converter models ensures their simulation with acceptable accuracy up to a switching frequency of around 1 kHz. Future hardware and software upgrades will soon allow the RT simulation of converters with substantially higher switching frequencies, without the loss of system complexity, at time steps around 1 μs.

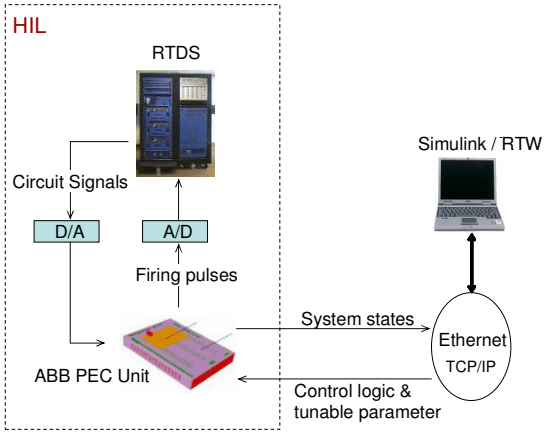


Fig. 4. HIL setting up

IV. Case Study 1: A Selective Shunt Active Filter

A. System Description

To cancel the harmonics produced by the nonlinear loads in the power distribution system, a selective shunt active filter (AF) is proposed using an adaptive method. This algorithm was first introduced by Bodson in [13] and [14] to cancel periodic acoustic disturbances of unknown frequencies. However, here this method is used and extended in the application of a shunt active filter.

The active filter injects compensating currents i_{AF}, of equal amplitude but opposite phase, at the point of grid connection to cancel the harmonics currents or reactive power caused by the nonlinear load. In this section, only harmonic cancellation is considered.

B. Control Structure

The control topology is shown in Fig. 5 where $i_{Load}(t)$ is the load current measured, $i_{Estimate}(t)$ is the estimate of the load current, $i_i(t)$ is the estimate of the fundamental or harmonic current ($i = 1,3,5...,n$) and α_1 is the estimate phase angle of the fundamental current. The objective is to make $i_{Load} - i_{Estimate}$ approach zero as time approaches infinity.

For the application of harmonic selective cancellation, the estimated harmonics $i_i(t)$ $(i = 3,5,7...)$ are used as the reference signal to the AF to generate the compensating currents opposite in phase to cancel the specific harmonics. In an ideal situation, after some time, the estimate of the specific harmonics should be nearly zero. This feature can be used to eliminate specific harmonics leading to the improvement in power quality. So the adaptive method is flexible and simple.

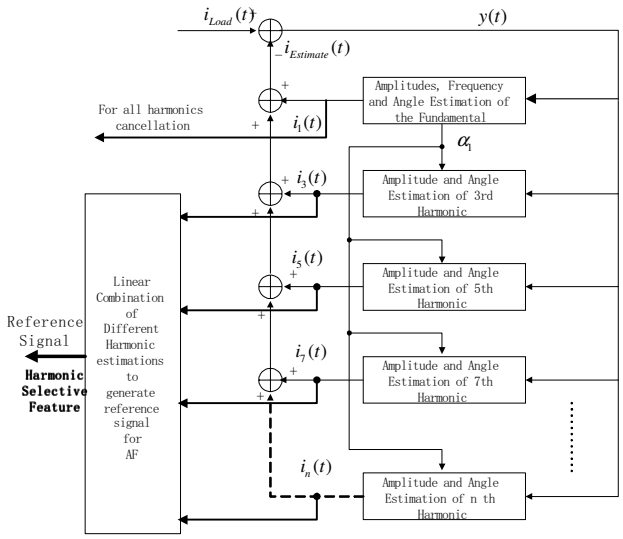


Fig. 5. Control Structure of the Proposed AF

C. Simulation

The proposed algorithm is applied to a single-phase shunt active filter to verify the algorithm. The simulation uses both the MATLAB and the PSIM simulating environments. The simplified block diagram of the test system is shown in Fig.6. The test system consists of a single phase AC source with a nonlinear diode bridge load. The active filter is connected parallel to the nonlinear load. The load current measured by the current sensor is sent to the adaptive algorithm module. This module obtains the information about the fundamental and harmonic components of the load current. The identified harmonic current signal is used as the reference signal for active filter control.

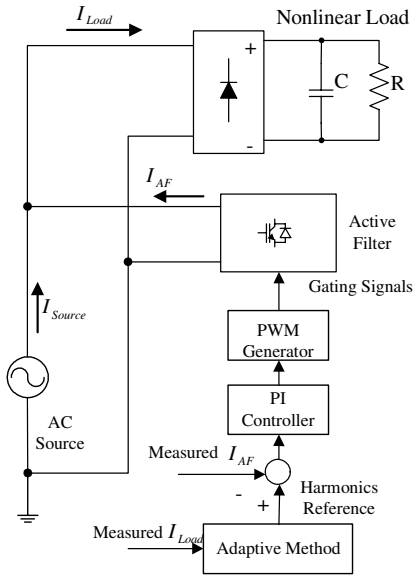


Fig. 6. Simplified Simulation Implementation Block Diagram

For current tracking purpose, the reference signal is compared with the output current of the active filter to generate the error signal. This error signal is passed through a PI controller to get the modulation signal for the PWM generator. The PWM generator outputs the gating signals for the active filter and the compensating current is therefore generated and sent to the AC bus for harmonic cancellation.

When there is no active filter control, the source current has the same waveform as the load current as shown in Fig.7. From Fig.7, we can clearly see that the source current is greatly distorted. From the spectrum analysis of the source current, in Fig.8, we can find significant 3rd and 5th harmonics there. The THD of the source current without active filter control is 29.43%.

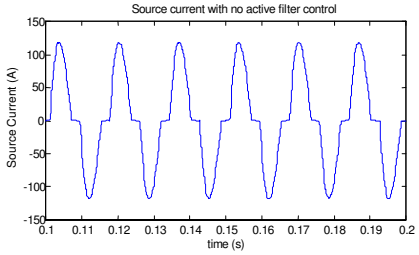


Fig. 7. Source current waveform without active filter control

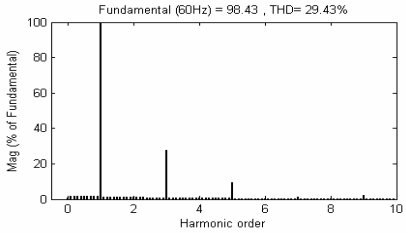
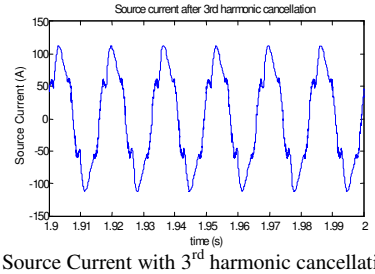
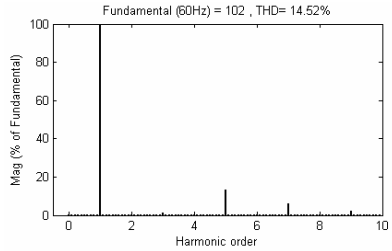


Fig. 8. Spectrum analysis of the source current

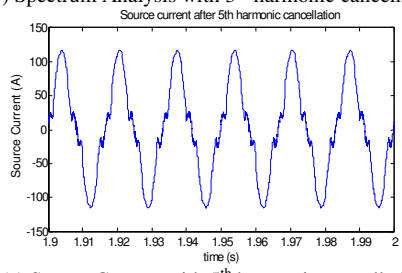
First, the 3rd harmonic cancellation is applied, and then the 5th harmonic cancellation is simulated. Fig.9 shows the simulation results of the source current with different harmonic cancellations. Fig.9 (a) and (c) shows the source current waveforms with 3rd and 5th harmonic cancellation, respectively. It is clearly seen that the source currents are shaped to match the sinusoidal waveforms. The spectrum analysis of the source currents under different harmonic cancellation applications is shown in Fig. 9 (b) and (d). Fig. 9 (d) clearly demonstrates that the 3rd harmonic is cancelled and the Total Harmonic Distortion (THD) factor is reduced to 14.52%. Fig 9 (d) shows that the 5th harmonic is cancelled and the THD reduces to 22.76%.



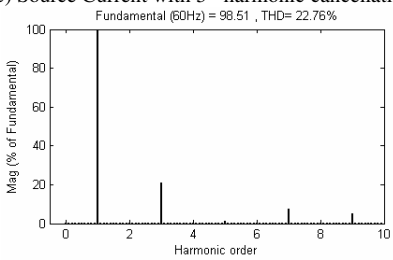
(a) Source Current with 3rd harmonic cancellation



(b) Spectrum Analysis with 3rd harmonic cancellation



(c) Source Current with 5th harmonic cancellation



(b) Spectrum Analysis with 5th harmonic cancellation

Fig. 9. Simulation Results of source current with the Proposed Active Filter

The simulation results show that the adaptive method is effective in reducing the specific harmonics in the power network. The adaptive algorithm proposed here is very simple and it only requires the measured load current thereby simplifying the control block.

V. Case Study 2: A Simplified Static Synchronous Compensator (StatCom)

In this section, a RT-HIL simulation of a 100 kVA STATCOM is realized. Several assumptions are made for the simplified distribution system. The objectives of the control are: first, to keep the DC link voltage constant and second, to compensate the reactive power consumed by other load on the grid so that the power factor can be improved.

A. System description and control block diagram

A system similar to that in Fig. 10 (a) was implemented in RTDS. The front-end rectifier of the PEBB-based motor drive is controlled from the external UC (AC 800-PEC). The simulated DC bus voltage U_{dc}, the three-phase grid voltage (U_{123}) and current (I_{123}), and the reactive power consumed on the grid (Q) are transmitted from RTDS to the UC via D/A channels. The UC generates appropriate firing pulses and sends them back to the RTDS In a closed loop arrangement as illustrated earlier in Fig. 4.

Fig. 10 (b) illustrates the control algorithm according to [12] which has been implemented on the UC. The outer DC bus voltage loop and reactive power loop compute the command d and q axis currents respectively. In the much faster inner current loop, command currents are compared with actual values to generate reference PWM voltage. The coupling effect between the two-axis currents is taken into account by the ωL branch. A ωC_f feed forward path is added to compensate for the shunt current due to the filter capacitors.

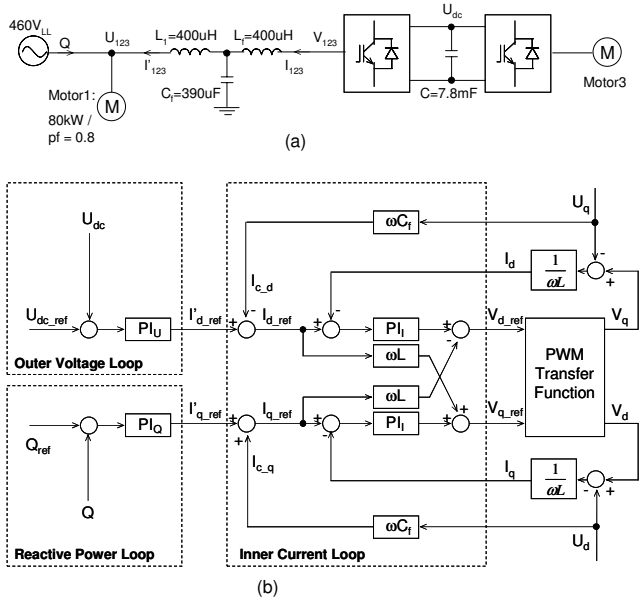


Fig. 10. (a) Simplified circuit; (b) two-loop control block diagram for STATCOM (front end rectifier of the motor drive)

B. Simulation Result

Two sets of simulations were performed to test the control algorithm and the HIL setup: first, the control algorithm was verified by off-line simulation where the firing pulses come from an implementation of the controls in RTDS. Second, that same control algorithm was then implemented on the UC and tested in the RT-HIL experiment. Fig. 11 plots representative simulation results. The U_{dc} reference steps from 0.9 kV to 0.7 kV at about 0.25 s and back to 0.9 kV at around 1.3 s. The step response from the RT-HIL simulation matches very well with that from the pure software simulation. The good agreement provides additional confidence in the HIL experimental setup and in the proper implementation of the control algorithm on the UC platform.

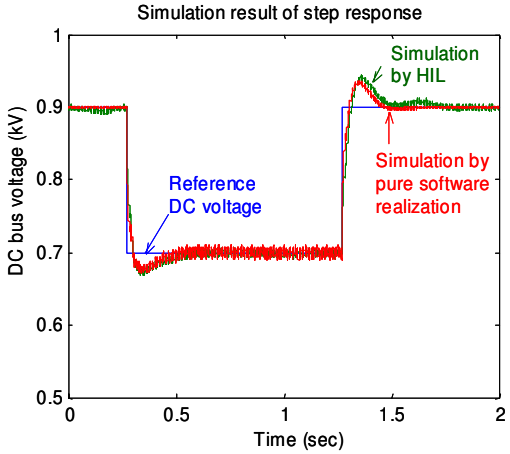


Fig. 11 Comparison of complete software and RT-HIL simulation results

Finally, Fig. 12 illustrates the functionality of the SATACOM controls. The firing of STATCOM is activated at 0.1 s and as a result the reactive power demand from the grid connection drops to zero accordingly. A transient increase in the active power is due to building up of the DC link voltage.

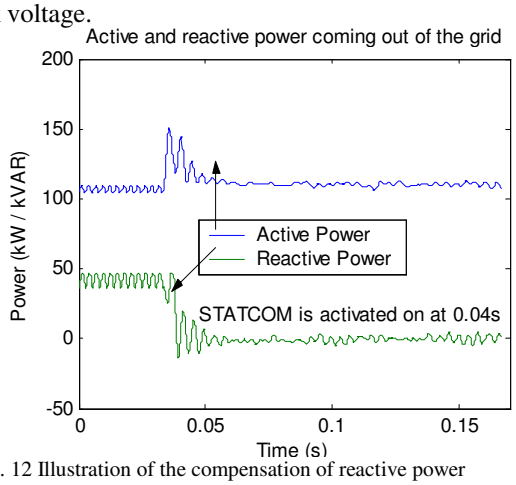


Fig. 12 Illustration of the compensation of reactive power

VI. Conclusions and Future Works

In this paper, RT-HIL simulation is proposed to augment the development of functional reconfiguration of PEBB and UC. Two cases, which represent two common applications of a PEBB based power converter, were studied. The reconfiguration of a PEBB/UC from a motor drive in a military all-electric-ship to an active filter was demonstrated in software simulation only. In the second case, the Real Time Digital Simulator was utilized to emulate the PEBB converter and its associated power system. The corresponding control algorithm was tested by means of HIL.

It is concluded that the RT-HIL method expedites the design, implementation, and testing of different control strategies substantially. First, RT-HIL includes the entire controller hardware and software, not only the control algorithm, in a virtual system environment. The effectiveness and stability of the controller can be studied with the additional aspect of real-time signal transfers. Therefore, shortfalls or even defects in controller can be identified prior to connecting it to the real power electrical system. Second, faster controller tuning becomes possible since, for example, certain hardware such as the FPGA modulator does not need to be simulated.

In the future, improvement to the RT-HIL environment should include parameter communication between the simulator and the UC for batch mode controller optimization. With respect to functional reconfiguration of PEBBs, requirements on passive components, sensing and instrumentation, as well as converter losses should be addressed more rigorously.

VII. References

[1] N. G. Hingorani, "Power Electronics Building Block Concepts," IEEE Power Engineering Society General Meeting 2003, vol. 3, 13-17 July 2003, pp. 1339-1343.

[2] T. Ericsen, A. Tucker, "Power Electronics Building Blocks and Potential Power Modulator Applications", 23rd Power Modulator Symposium, 1998, 22-25 June 1998, pp. 12-15.

[3] P. K. Steimer, "Power Electronics Building Blocks – a Platform-based Approach to Power Electronics," IEEE Power Engineering Society General Meeting, July 2003, vol. 3, pp. 1360-1365.

[4] D. Maclay, "Simulation Gets into the Loop," IEE Review, Vol. 43, No. 3, May 1997, pp. 109-112.

[5] P. Terwiesch, T. Keller, E. Scheiben, "Rail Vehicle Control System Integration Testing Using Digital Hardware-in-the-Loop Simulation," IEEE Transactions on Control Systems Technology, Vol. 7, No. 3, May 1999, pp. 352-362.

[6] A. J. Grono, "Synchronizing Generators with HITL Simulation," IEEE Computer Applications in Power, Vol. 14, No. 4, October 2001, pp. 43-46.

[7] S. Ayasun, S. Vallieu, R. Fischl, T. Chmielewski, "Electric Machinery Diagnostic/Testing System and Power Hardware-in-the-Loop Studies," Symposium on Diagnostics for Electric Machines, Power Electronics and Drives 2003, Atlanta, GA, USA, August 2003, pp. 361-365.

[8] Y. Liu, M. Steurer, S. Woodruff, P. R. Ribeiro, "A Novel Power Quality Assessment Method Using Real Time Hardware-in-the-Loop simulation," 2004 International Conference on Harmonics and Power Quality (accepted).

[9] P. K. Steimer, "Power Electronics Building Blocks – a Platform-based Appproach to Power Electronics," Power Engineering Society General Meeting, 2003, IEEE, Vol. 3, 13-17, July 2003.

[10] ABB Switzerland Ltd., "Control AC 800PEC, Controller Hardware Product Guide -- Draft", 2003

[11] RTDS technologies, "Real-Time Digital Simulator Hardware Manual", Manitoba, Canada, 2001

[12] Vladimir Blasko, Vikram Kaura, "A New Mathematical Model and Control of a Three-Phase AC-DC Voltage Source Converter", IEEE Transactions on Power Electronics, Vol. 12, No. 1, January 1997, 116-123.

[13] M. Bodson, J. S. Jensen, S. C. Douglas, "Active Noise Control for Periodic Disturbances", IEEE Transactions on Control Systems Technology, Vol. 14, No. 4, January 2001, pp. 200-205.

[14] M. Bodson, S. C. Douglas, "Adaptive Algorithms for the Rejection of Sinusoidal Disturbances with Unknown Frequency", Automatica, Vol.33, No.12, 1997, pp.2213-2221