Nonlinear Control of Buck-Boost AC/DC Converters: Output Voltage Regulation & Power Factor Correction

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Abstract— **We are considering the problem of controlling *AC/DC* switched power converters of the *Buck-Boost* type. The control objectives are twofold: (i) regulating the output voltage to a desired reference value, (ii) assuring a unitary power factor by enforcing the voltage and the current delivred by the electric network to be in phase. The considered problem is dealt by designing a *cascade-structure nonlinear* controller. The inner loop of the latter regulates the active power provided by the network; it is built-up using the backstepping design approach. The outer loop regulates the converter squared output voltage using a PI regulator; such a simple solution is made possible using adequate model transformations and loop operation mode separation. The controller thus obtained is shown to achieve the control objectives and proves to be robust with respect to load changes.**

I. INTRODUCTION

THE static power converters have a very wide domain of applications. However, these converters still have an important drawback as they contribute to the pollution of the electric network. Therefore, converter controllers should not only have as objective output voltage regulation, but also rejection of the current harmonics. Surprisingly enough, most of previous works have focussed only on voltage regulation [1]-[5]. In fact, these works have generally based their studies only on the DC/DC part of the converters i.e., the rectifier ensuring the connection to the network has been ignored.

In the present paper, we are considering the problem of controlling a whole AC/DC converter. We will particularly focus on AC/DC converters with back-boost chopper (Fig.2.1). Our objective is to regulate the output voltage while ensuring a unitary power factor (PF). To deal with the considered control problem a nonlinear controller including two loops is built-up.

The inner loop is first developed in such a way that the converter input current be sinusoidal and in phase with the network supply voltage. So doing, the objective of current harmonics rejection is achieved. The regulator involved in the inner loop is designed by the backstepping technique that accounts for the systems dynamics nonlinearity. The converter variable-structure feature is coped with basing the above regulator design upon an average model of the system. It is worth noting, that averaging is widely used in the literature [6]-[8].

The natural purpose of the outer loop would be the regulation of the converter output voltage vo. However, we will choose to perform regulation of v_o^2 rather than vo. Actually, v_o^2 undergoes a (first-order) linear differential equation while vo undergoes a nonlinear equation. Using this variable transformation ($vo \rightarrow v_o^2$), as well as an ad-hoc loop operation mode separation, reference tracking on v_o^2 can be achieved using a simple PI regulator.

A theoretical analysis, involving Lyapunov stability tools, shows that the nonlinear cascade controller thus constructed actually achieves its objectives (harmonics rejection and voltage regulation). The controller performances and robustness are further illustrated by many simulated examples.

The paper is organized as follows: in Section II, the Buck-Boost converter is described and modeled; Section III is devoted to designing the inner loop, using the backstepping technique, and the synthesis of the outer loop. the controller performances are illustrated by simulations in Section IV; a conclusion and a reference list end the paper.

II. MODELLING OF THE CONVERTER

The AC/DC Buck-Boost converter under study is represented by Fig. 2.1. It includes three main parts, namely a LC-filter, a diode bridge rectifier and a buck-boost chopper. The latter operates according to the so-called Pulse Width Modulation (PWM) principle, [2]-[3]. This means that time is shared in intervals of length T. Within any period, the IGBT-switch is ON during αT, for some $0 \leq \alpha \leq 1$. Then, energy is stored in the inductance Lo and the diode Do is blocked. During the rest of the period, i.e. $(1-\alpha)T$, the switch IGBT is OFF and, consequently, the inductance discharges in the load resistance Ro. The value of α varies from a period to an other and its time-variation law determines the trajectory of output voltage vo. Then,

the variable α, which is called duty cycle, turns out to be the control input for the converter.

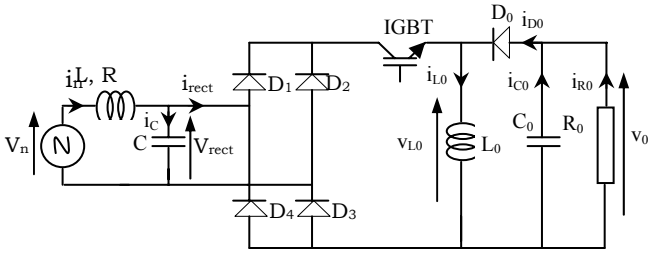

Fig. 2.1: converter AC/DC buck-boost

Mathematical modeling of the converter is completed applying Kirchhoff's laws. So doing, one gets the following equations:

$$v_n = R.i_n + L\frac{di_n}{dt} + v_{rect} \quad (2.1)$$

$$i_n = C\frac{dv_{rect}}{dt} + i_{rect} \quad (2.2)$$

$$v_{Lo} = L_o\frac{di_{Lo}}{dt} \quad (2.3)$$

$$i_{Do} = -C_o\frac{dv_o}{dt} - \frac{v_o}{R_o} \quad (2.4)$$

The current i_{rect} takes undergoes different equations depending on the state of the IGBT-switch. These equations can be given a unique mathematical expression by introducing a binary variable μ=1 if IGBT is ON and μ=0 if IGBT is OFF. Then, one has for i_{rect} the following expressions:

$$i_{rect} = \mu.\mathrm{sign}(v_{rect})i_{Lo} \quad (2.5)$$

Similarly, the current iDo in the diode Do undergoes different laws, depending on the states of the diode and the IGBT-switch.These laws can be given a unique mathematical expression by introducing a binary variable λ:

$$\lambda = 1 \quad si \quad i_{Lo} > 0 \quad \text{and} \quad \lambda = 0 \quad si \quad i_{Lo} \le 0 \quad (2.6)$$

Then, one gets the following expression for i_{Do}:

$$i_{Do} = \lambda(1-\mu)i_{Lo} \quad (2.7)$$

The inductor voltage v_{Lo} also depends on the states of the IGBT-switch and the diode D_o. It is given by:

$$v_{Lo} = \mu|v_{rect}| + \lambda(1-\mu)v_o \quad (2.8)$$

Substituting (2.5), (2.7) and (2.8) in (2.1)-(2.4), yields the final form of the (instantaneous) converter model:

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$$\frac{di_n}{dt} = -\frac{R}{L}i_n - \frac{v_{rect}}{L} + \frac{v_n}{L} \quad (2.9a)$$

$$\frac{dv_{rect}}{dt} = \frac{i_n}{C} - \mu\frac{\mathrm{sign}(v_{rect})}{C}i_{Lo} \quad (2.9b)$$

$$\frac{di_{Lo}}{dt} = \mu\frac{|v_{rect}|}{L_o} + \lambda\frac{(1-\mu)}{L_o}v_o \quad (2.10a)$$

$$\frac{dv_o}{dt} = -\lambda\frac{(1-\mu)}{C_o}i_{Lo} - \frac{v_o}{R_oC_o} \quad (2.10b)$$

This model is useful to build-up an accurate simulator for the converter. However, it cannot be based upon to design a continuous control law as it involves a binary control input, namely μ. To overcome this difficulty, it is usually resorted to the averaging process over cutting intervals, [6]-[8]. This process is shown to give rise to average versions (of the above model) involving as a control input the mean value of μ which is nothing other than the duty cycle α. Supposing the converter operating in continuous conduction mode, the average model turns out to be the following:

$$\frac{di_n}{dt} = -\frac{R}{L}i_n - \frac{v_{rect}}{L} + \frac{v_n}{L} \quad (2.11a)$$

$$\frac{dv_{rect}}{dt} = \frac{i_n}{C} - \alpha\frac{\mathrm{sign}(v_{rect})}{C}i_{Lo} \quad (2.11b)$$

$$\frac{di_{Lo}}{dt} = \alpha\frac{|v_{rect}|}{L_o} + \frac{(1-\alpha)}{L_o}v_o \quad (2.12a)$$

$$\frac{dv_o}{dt} = -\frac{(1-\alpha)}{C_o}i_{Lo} - \frac{v_o}{R_oC_o} \quad (2.12b)$$

where we have used the fact that $\lambda = 1-\mu$ because of the continuous conduction mode. Equations (2.11a-b)-(2.12a-b) show that the converter average dynamics are nonlinear.

III. CONTROLLER DESIGN

Our aim is to design for the AC/DC Buck-Boost converter a controller that ensures both power factor correction (PFC) and output voltage regulation. The controller synthesis will be performed in two major steps. First, a current inner loop is designed to cope with the PFC issue. In the second step, an outer voltage loop is built-up to achieve output voltage regulation.

A. Current inner loop design

The PFC objective means that the converter input current should be *sinusoidal* and *in phase* with the network supply voltage. We therefore seek a regulator that enforces the current i_n to track a reference signal of the form $i_{nref} \overset{def}{=} K\,v_n$. At this point the parameter K is any real number. The regulator will now be designed using the backstepping technique [9], based on the (partial) model (2.11a-b).

Let us introduce the following tracking error on the current:

$$e = i_n - i_{nref} \quad (3.1)$$

Using (2.11a), time-derivation of (3.1) yields the following error dynamics:

$$\frac{de}{dt} = -\frac{R}{L} i_n - \frac{v_{rect}}{L} + \frac{v_n}{L} - \frac{di_{nref}}{dt} \qquad (3.2)$$

In (3.2), $\left(\frac{v_{rect}}{L}\right)$ stands as a (virtual) control variable. Then, e can be regulated to zero if $(v_{rect}/L) = (v_{rect}/L)_{ref}$ with:

$$\left(\frac{v_{rect}}{L}\right)_{ref} = -\frac{R}{L} i_n + \frac{v_n}{L} - \frac{di_{nref}}{dt} + k_e e \qquad (3.3)$$

(k_e any positive real constant) (3.3)

Indeed, this choice would imply that: $\dot{e} = -k_e e$. The corresponding Lyapunov function V_1 and its derivative $\dot{V}_1$ are given by:

$$V_1 = 0.5e^2 \quad \text{and} \quad \dot{V}_1 = -k_e.e^2 \qquad (3.4)$$

As $\left(\frac{v_{rect}}{L}\right)$ is not the actual control input, a new error variable z is introduced :

$$\begin{aligned} z &= \left(\frac{v_{rect}}{L}\right) - \left(\frac{v_{rect}}{L}\right)_{ref} \\ &= \left(\frac{v_{rect}}{L}\right) + \frac{R}{L} i_n - \frac{v_n}{L} + \frac{di_{nref}}{dt} - k_e e \end{aligned} \qquad (3.5)$$

Then, equations (3.2)-(3.4) become:

$$\frac{de}{dt} = -k_e e - z \quad , \quad \dot{V}_1 = -k_e.e^2 - ez \qquad (3.6)$$

Now, time-derivation of z gives, using (2.11a-b) and (3.5):

$$\begin{aligned} \frac{dz}{dt} &= \frac{i_n}{LC} - \alpha \frac{sign(v_{rect})}{LC} i_{L0} - \frac{R^2}{L^2} i_n \\ &\quad - \frac{R}{L^2} v_{rect} + \frac{R}{L^2} v_n - \frac{1}{L} \frac{dv_n}{dt} \\ &\quad + \frac{d^2 i_{nref}}{dt^2} + k_e^2 e + k_e z \end{aligned} \qquad (3.7)$$

Notice that the actual control variable, namely α, appears for the first time in equation (3.7). An appropriate control law for generating α, has now to be found for the system (3.6)-(3.7) whose state vector is (e, z). To this end, let us consider the Lyapunov candidate function V_2 :

$$V_2 = 0.5e^2 + 0.5z^2 \qquad (3.8)$$

Its time-derivative along the (e, z) trajectory (equations (3.6)-(3.7)), yields:

$$\dot{V}_2 = -k_e e^2 - k_z z^2 - z(e - \dot{z} - k_z z) \qquad (3.9)$$

This shows that, for the (e, z)-system to be globally asymptotically stable, it is sufficient to choose the control α so that $\dot{V}_2 = -k_e e^2 - k_z z^2$ which in view of (3.9) amounts to ensuring that:

$$\dot{z} = e - k_z z \qquad (3.10)$$

Replacing in (3.10) $\dot{z}$ by its expression (3.7) and solving the resulting equation with respect to α, yields the following backstepping control law:

$$\begin{aligned} \alpha = \frac{sign(v_{rect})}{i_{L0}} \Bigg\{ & \left(1 - \frac{R^2 C}{L}\right) i_n + \frac{RC}{L}(v_n - v_{rect}) \\ & - C\frac{dv_n}{dt} + LC(K_e^2 - 1)e + LC(k_e + k_z)z + LC\frac{d^2 i_{nref}}{dt^2} \Bigg\} \end{aligned} \qquad (3.11)$$

$$i_{nref} \overset{def}{=} K v_n \qquad (3.12)$$

Proposition 3.1. Consider the system, next called *inner closed-loop*, consisting of the subsystem (2.11a-b) and the control law (3.1), (3.5) (3.11) and (3.12). Let us assume that the ratio K is bounded and the derivatives $\frac{di_{nref}}{dt}$ and $\frac{d^2 i_{nref}}{dt^2}$ are available. Then, the closed loop system errors ($e=i_n-i_{nref}$ and z) are globally asymptotically vanishing. More precisely, these undergo the following equation:

$$\frac{d}{dt}\begin{pmatrix} e \\ z \end{pmatrix} = \begin{pmatrix} -k_e & -1 \\ 1 & -k_z \end{pmatrix} \begin{pmatrix} e \\ z \end{pmatrix} \qquad (3.13)$$

where the design parameters k_e and k_z are arbitrary positive real numbers.

Remarks 1.

1) The control law (3.11) involves, in one hand, the derivative $\frac{dv_n}{dt}$ which is available (since the network voltage is a known sinusoid) and, in the other hand, the derivatives $\frac{di_{nref}}{dt}$ and $\frac{d^2 i_{nref}}{dt^2}$.

2) The control law (3.12) is illustrated by figure 3.2.

B. Outer voltage loop design

The aim of the outer loop is to generate a tuning law for the ratio K in such a way that the output voltage vo be regulated to a given reference value voref. The first step in designing such a loop is to establish the relation between the ratio K (control input) and the output voltage vo. This is the object of the following proposition.

Proposition 3.2. Consider the inner closed-loop system (consisting of the subsystem (2.11a-b) and the control law (3.1), (3.5), (3.11) and (3.12) together with the subsystem (2.12a-b).

1°) The output voltage v_o varies in response to the tuning ratio K according to the following equation:

$$\frac{dv_o}{dt} = -\frac{v_o}{R_o C_o} - \frac{\hat{v}_n^{\,2}}{2Cov_o}\left(1 - \cos(2\omega_n t)\right)K \qquad (3.14)$$

where $\hat{v}_n$ denotes the magnitude of the network (sinusoidal) voltage v_n.

2°) the squared output voltage v_o^2 varies in response to the tuning ratio K according to the following equation:

$$\frac{dy}{dt} = -\frac{2}{R_o C_o} y + \frac{\hat{v}_n^{\,2}}{C_o}\left(1-\cos(2\omega_n t)\right)K \qquad (3.15)$$

Proof. 1) The first step consists in replacing the circuit part above the set C_o-R_o, by an equivalent current generator, as shown by Fig. 3.1. In view of equation (2.12b), the underlying current value i_{equ} coincides with $(1-\alpha)i_{Lo}$. So, (2.12b) becomes:

$$\frac{dv_o}{dt} = -\frac{i_{equ}}{C_o} - \frac{v_o}{R_o C_o} \qquad (3.16)$$

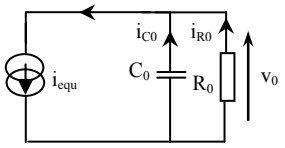

Fig. 3.1 : equivalent current generator

The equivalent current i_{equ} will now be expressed in function of the tuning ratio K, using power conservation arguments. The instantaneous power at the converter input is given by:

$$P_n = k\hat{v}_n^2 \sin^2(\omega_n.t) = \frac{K\hat{v}_n^2}{2}\left(1-\cos(2\omega_n.t)\right) \qquad (3.17)$$

On the other hand, the power that is actually transmitted to the load is $P_{load} = -v_o i_{equ}$. the instantaneous power at the input is integrally transmitted to the load (dissipative element). Then, the quantity Pload does coincide with Pn, which implies that: $i_{equ} = -K\frac{\hat{v}_n^2}{2v_o}\left(1-\cos(2\omega_n t\right)$, which together with (3.16) establishes (3.14).

2) Equation (3.14) shows that the relation between the variable K and the output voltage v_o is nonlinear and (periodically) time-varying. The nonlinear feature can be coped with by operating the following variable change $y = v_o^2$ in (3.14). Actually, deriving y with respect to the time and using (3.14), yields the first-order linear model (3.15) and completes the proof of Proposition 3.2.

The main drawback of model (3.15) is the fact that it is time-varying and, in particular, is uncontrollable as the term $(1-\cos(2\omega_n t))$ periodically vanishes. Such an issue can be coped with supposing the controller loops to operate in completely separated modes: fast operating mode for inner loop and slow mode for the outer. This formally amounts to supposing that the power spectra of the signal K is sufficiently small, for $\omega \geq \omega_B$ where $\omega_B = \frac{\omega_n}{10}$ and $\omega_n = 2\pi.50 = 100\pi$ (rd/sec).

Now, let F(s) be any low-pass filter that rejects, particularly, the frequency $2\omega_n = 200\pi$ rd/sec. Such a filter may be a simple second-order Butterworth type:

$$F(s) = \frac{1}{1+2\xi\frac{s}{\omega_n}+\frac{s^2}{\omega_n^2}} \quad \text{with} \quad \xi = \frac{1}{\sqrt{2}} \qquad (3.18)$$

Given the frequency nature of K, an immediate consequence of (3.18) is that: F(s)[K]≅K. Then, operating F(s) on both sides of (3.15) yields:

$$\frac{dy_f}{dt} = -\frac{2}{R_o C_o} y_f + \frac{\hat{v}_s^{\,2}}{C_o} K \qquad (3.19)$$

where y_f=F(s)[y] denotes the filtered version of y. The filtered model thus obtained, is both time-invariant and controllable.

Based on the above first-order time-invariant linear model a simple PI regulator, $C(s) = k_p + \frac{k_i}{s}$, can be used to ensure the convergence to zero of the tracking error y_f-y^*, where y^* is the desired reference for y_f. The underlying control law is then $K = C(s)(y^* - y_f)$.

Let G(s) denotes the transfer function of the filtered model (3.19) i.e. y_f=G(s)[K]

$$G(s) = \frac{k_o}{1+\tau_o s} \quad \text{with } \tau_o = \frac{R_o C_o}{2} \text{ and } k_o = \frac{R_o \hat{v}_n^{\,2}}{2}$$

It can be easily checked that the closed loop system including the subsystem (3.14) and the control law $K = C(s)(y^* - y_f)$, has the following transfer function:

$$H(s) = \frac{C(s)G(s)}{1+C(s)G(s)} = \frac{1+\frac{k_p}{k_i}s}{1+(\frac{k_p}{k_i}+\frac{1}{k_i k_o})s+\frac{\tau_o}{k_i k_o}s^2} \qquad (3.20)$$

Given desired values of the damping factor ξ_d>0 and natural frequency ω_d. Then, the regulator parameters will be chosen so that:

$$\frac{k_p}{k_i}+\frac{1}{k_i k_o} = \frac{2\xi_d}{\omega_d} \quad \text{and} \quad \frac{\tau_o}{k_i k_o} = \frac{1}{\omega_d^2} \qquad (3.21)$$

This end up the whole controller design which performances are described in the following Theorem.

Theorem (main result). Consider the AC/DC Buck-Boost power converter shown by Fig. 2.1 in closed-loop with the controller consisting of the inner-loop regulator (3.11)(3.12) and the outer-loop regulator defined by the control law $K = C(s)[y^* - y_f]$ with y_f=F(s)[y], $C(s) = k_p + \frac{k_i}{s}$ where F(s) and (k_p, k_i) are given by (3.18) and (3.21), respectively.

Let the reference signal y* be the filtered version of v_{oref}^2, through any low-pass second order filter, where

voref denotes the bounded reference value for the output voltage vo. More precisely, y*=F*(s)[v_{oref}^2] and F*(s) may be a second order Butterworth type whose band-pass is let to the designer choice. Furthermore, the filtering operation yielding y* will be made precise later,

Finally, let us suppose that the power spectra of (outer-loop control signal) K is sufficiently small for $\omega \geq \omega_B$, so that mode separation is achieved. Then, the resulting closed-loop system has the following properties:

1) all signals of remain bounded,

2) $i_n - i_{nref}$ vanishes asymptotically,

3) if v_{oref} is step signal then $(y^* - y_f)$ vanishes asymptotically.

Remark 2.

a) The fact that the spectrum of signal K be limited to the frequency $\omega_B = \frac{\omega_n}{10}$, means that K is too slow compared to the signal cos($2\omega_n$). Then, comparing equations (3.15) and (3.19), it follows that the squared output voltage $y = v_o^2$ will asymptotically oscillates, at frequency $2\omega_n$, around y_f.

b) The control system described in the above Theorem is illustrated by Fig. 3.2.

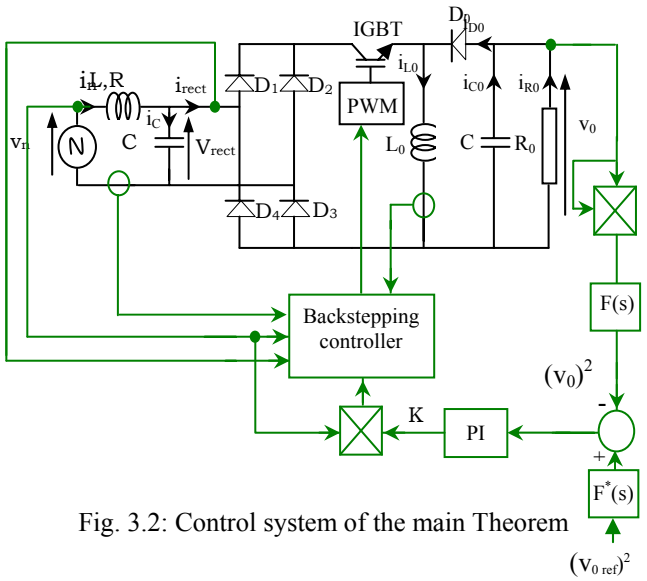

Fig. 3.2: Control system of the main Theorem

IV. SIMULATIONS

Performances and design aspects of the controller developed in the previous section will now be illustrated by simulations performed in the Matlab/Simulink environment. The controlled AC/DC converter has the following characteristics: $\hat{v}_n = 60V$, R=0.01Ω, L=2mH, C=10μF, L_o=20mH, C_o=4000μF, R_o=20Ω and it operates at the cutting frequency $f_{=10}$kHz.

The reference squared output voltage v_{oref}^2 is a step signal of amplitude 2500 (Volts)^2. An adequate choice for the reference filter turned out to be

$$F^*(s) = \frac{1}{1 + (2\xi / 2\omega_n)s + (1/2\omega_n)^2 s^2}$$

The values k_e = 10000 and k_z = 15000 proved to be appropriate for the inner loop design parameters.

Bearing in mind Remark 2a, the outer loop parameters have been chosen as follows: $\xi_d = 0.7$ and $\omega_d = 10\pi$ (rd/sec). These yield a filter $C(j\omega)/(1 + C(j\omega)G(j\omega))$ whose Bode diagram is shown by figure 4.1. As the corresponding pass band is nearly [0, ω_B], the loop mode separation is achieved (Remark 2a).

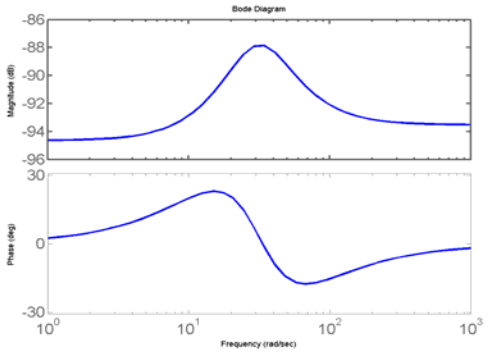

Fig. 4.1: Bode diagram (signal K)

Fig. 4.2 to Fig. 4.5 illustrates the controller performances. As expected (Remark 2b), both v_o^2 and v_o converge in the mean to their reference value (see Fig. 4.2 and Fig. 4.3). Furthermore, it is checked that the observed voltage ripple oscillate at the frequency $2\omega_n$.

(Remark 2b) and is much smaller than the average value of the signals.

Comparing Fig. 4.2 and 4.4, one particularly sees that the magnitude variation of the input current i_n is correlated to the (mean) value of the squared output voltage v_o^2. This confirms the power conservation through the circuit (as all elements are non-dissipative).

Fig. 4.5 shows that the outer-loop control K is practically unaffected by the ripple phenomena This confirms the mode separation between the inner and outer loop. Finally, Fig. 4.6 shows that the input current i_n and the output voltage v_o are in phase, ensuring a unitary power factor. The corresponding inner-loop control signal α is shown by Fig 4.7

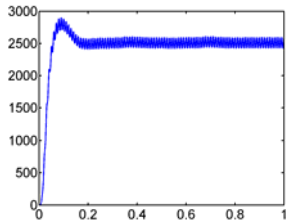

Fig. 4.2: squared voltage

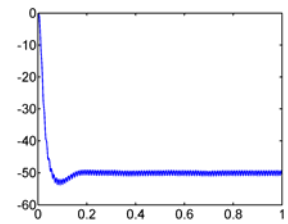

Fig. 4.3: output voltage v_o

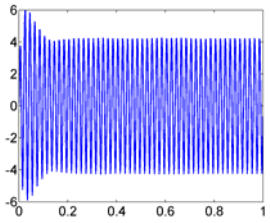

Fig. 4.4: current i_n

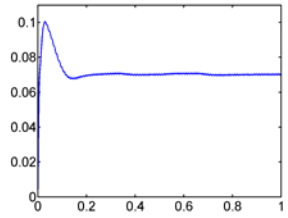

Fig. 4.5: singal K

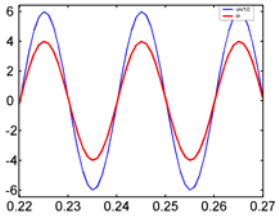

Fig. 4.6: v_n and i_n

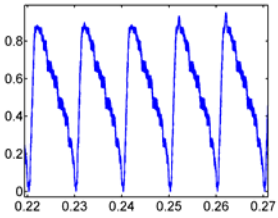

Fig. 4.7: control law α

To analyze the robustness capability of the proposed controller, a new experiment will be performed. It consists in changing the load resistance according to Fig. 4.10. Except for this change, the rest of the converter characteristics are the same as previously. The resulting closed-loop system behavior is illustrated by Fig. 4.11 to 4.13 The first figure shows that the effect of the resistance changes on the output voltage is well compensated by the controller. Fig. 4.12 shows that the PFC property is preserved despite the load variations. Finally, Fig. 4.13 shows that loop mode separation is still satisfied.

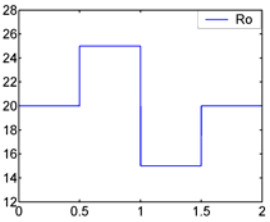

Fig. 4.10: Load resistance Ro

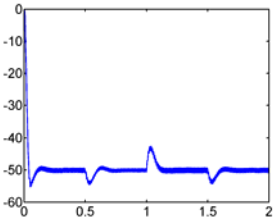

Fig. 4.11: voltage v_o

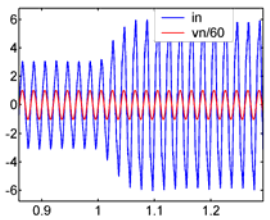

Fig. 4.12: current i_n and voltage v_n

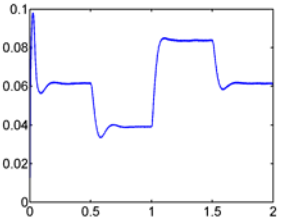

Fig. 4.13 : signal K

V. Conclusion

A new nonlinear controller is proposed for AC/DC Buck-Boost converters to achieve voltage output regulation and power factor correction. It is developed in two major steps. First, an inner-loop is designed, based on the backstepping technique, to ensure the PFC objective (that amounts to enforcing the input current i_n to be proportional to the voltage network v_n). The inner-loop regulator generates the duty cycle α so that the current i_n follow the reference $i_{nref}=Kv_n$, (Proposition 3.1). The second step consists in developing an outer-loop that generates the signal K so that the squared output voltage v_o^2 follows a given reference signal v_{oref}^2. The synthesis of this loop involves a linearizing variable change, a signal filtering to cope with model time-varying and controllability issues and a loop mode separation (Proposition 3.2).

A formal analysis (Main Theorem) and a simulation study prove that the proposed controller actually meets its objectives.

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