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Brief Paper

Sequential Design of Decentralized Controllers*†

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Key Words—Linear systems; decentralized control; controller design; robust control; structured singular value; PID controller.

Abstract—A procedure for sequential design of decentralized controllers for linear systems is presented. It is shown how to include a simple estimate of the effect of closing subsequent loops into the design problem for the loop which is to be closed. In the examples the robust performance in terms of the structured singular value is used as the measure of control performance, but the procedure may be applied also for other performance measures.

1. *Introduction*

DECENTRALIZED CONTROL REMAINS popular in the industry, despite developments of advanced controller synthesis procedures leading to full multivariable controllers.

The design of a decentralized control system consists of two main steps:

(1) control structure selection, that is, pairing inputs and outputs; and
(2) design of a single-input-single-output (SIO) controller for each loop.

In this paper we consider Step (2) and assume that Step (1) has already been completed, for example, by help of such tools as the RGA (Bristol, 1966; Hovd and Skogestad, 1992a,b).

A lot of the literature on decentralized control is concerned mainly with stability and uses of the time domain (e.g. Siljak, 1991). The focus in this paper is on design for performance where frequency-domain methods prove to be very useful.

Standard optimal controller synthesis algorithms (e.g. H_2 or H_∞ synthesis) lead to multivariable (centralized) controllers, and cannot handle requirements for controllers with a specified structure. Siljak (1991; p. 208) notes that despite a relatively long history, the optimization methods for decentralized control of stochastic systems are unsatisfactory. Recently, several parametrizations of all stabilizing decentralized controllers have been proposed (e.g. Manousiouthakis, 1989; Özgüler, 1990), but they are difficult to apply for synthesis. Date and Chow (1993) propose a two-stage design approach where in the first stage an H_2 or H_∞-centralized controller is obtained, and in the second step the parametrization of Manousiouthakis (1989) is used to optimize a parameter which decentralizes the controller. However, a fundamental problem is that the optimal decentralized controller is generally of infinite order (the "second guessing problem" as discussed by Sandell *et al.*, 1978).

Instead, some practical approaches to the design of decentralized controllers have evolved.

- Simultaneous design using parameter optimization for a fixed controller structure (e.g. Sandell *et al.*, 1978; Davison and Ferguson, 1981).
- Independent design (Skogestad and Morari, 1989).
- Sequential design (e.g. Mayne, 1973).

Simultaneous design using parameter optimization is very difficult numerically, and it does not provide some of the advantages that are usually the reason for using decentralized control in the first place, such as the ability to bring the system into service by closing one loop at a time, and the guarantee of stability in the case of failures. In the independent design procedure of Skogestad and Morari (1989), used also by Hovd and Skogestad (1993) and Braatz *et al.* (1992), the issue of interaction between the loops is considered first, and the SISO controllers are then designed independently, using bounds that guarantee stability and performance. The disadvantage is that performance may be poor because the method does not use detailed information about how the other loops are designed.

Luyben (1986) has proposed a simple procedure (called BLT) which is a combination of independent and simultaneous design, where all the loops are first tuned independently using the Ziegler-Nichols procedure, and then a common detuning factor is applied in order to take care of the interactions.

In this paper we discuss sequential design, which is probably the most common design procedure in real applications. In spite of this, there exist very few, if any, good design methods. In the paper we present a new design procedure based on obtaining simple a priori estimates of the final loop shapes.

In the example we use the structured singular value, introduced by Doyle (Doyle *et al.*, 1982), as the measure of control quality. However, the procedure can be applied also for other performance measures.

1.1. *Notation.* The matrix $G(s)$ denotes a square plant of dimension $n \times n$, and $g_{ij}(s)$ is the ijth element of $G(s)$. The decentralized controller is assumed to be diagonal with diagonal elements $c_i(s)$ (see Fig. 1). The matrix consisting of the diagonal elements of G is denoted $\tilde{G} = \text{diag}\{g_{ii}\}$. The sensitivity function is $S = (I + GC)^{-1}$ and the complementary sensitivity is $H = I - S = GC(I + GC)^{-1}$. Loop i is the SISO feedback system consisting of g_{ii} and c_i. The sensitivity functions and complementary sensitivity functions for the individual loops are collected in the diagonal matrices $\tilde{S} = \text{diag}\{\tilde{s}_i\} = \text{diag}\{1/(1 + g_{ii}c_i)\} = (I - \tilde{G}C)^{-1}$ and $\tilde{H} = \text{diag}\{\tilde{h}_i\} = \text{diag}\{g_{ii}c_i/(1 + g_{ii}c_i)\} = \tilde{G}C(I - \tilde{G}C)^{-1}$. Two frequency-dependent measures which we make use of are the Performance Relative Gain Array, PRGA $= \Gamma = \tilde{G}G^{-1}$ (with elements γ_{ij}), and the Closed-loop Disturbance Gain, CLDG $= \tilde{G}G^{-1}G_d$ (with elements δ_{ik}).

2. *Sequential design*

Sequential design involves closing and tuning one loop at a time. The method is very well suited for on-line tuning, but in this paper we explicitly make use of a process model (possibly uncertain) to improve the design.

The introduction of sequential design into the control literature is usually attributed to Mayne (1973), although he mainly considered precompensator design, and not the

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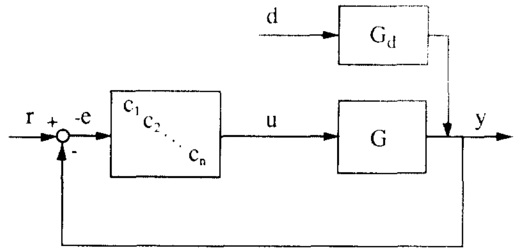

FIG. 1. Block diagram of feedback system with decentralized controller.

design of the decentralized controller. In any case it is probably fair to say that sequential design has always been the most popular design method for decentralized control of real multivariable processes. Relatively few theoretical results are available, although the method has attracted some attention more recently (e.g. Bernstein, 1987; Nett and Uthgenannt, 1988; Viswanadham and Taylor, 1988; Skogestad and Hovd, 1990; Chiu and Arkun, 1992).

2.1. *Advantages of sequential design*

1. Each step in the design procedure involves designing only one single-input–single-output (SISO) controller.
2. A limited degree of failure tolerance is guaranteed: if stability has been achieved after the design of each loop, then the system will remain stable if loops fail or are taken out of service in the reverse order of how they were designed.
3. Similarly, during startup the system will be stable if the loops are brought into service in the same order as they have been designed.

2.2. *Problems with sequential design*

1. The final controller design, and thus the control quality achieved, may depend on the order in which the controller in the individual loops are designed.
2. Only one output is usually considered at a time, and the closing of subsequent loops may alter the response of previously designed loops, and thus make iteration necessary.
3. The transfer function between input u_k and output y_k (which is considered when designing loop k) may contain right half-plane (RHP) zeros that do not correspond to RHP transmission zeros of $G(s)$.

The usefulness of a sequential design procedure will depend on how successfully it addresses the above issues. The conventional rule for dealing with problem 1 is to close the fast loops first, the reason being that the loop gain and phase in the bandwidth region of the fast loops is relatively insensitive to the tuning of the lower loops. While this argument is reasonable for loop k itself (involving only r_k, u_k and y_k), the response of output k may still be sensitive to the tuning of the controller in a slower loop l, if u_l has a large effect on y_k.

We will attempt to reduce the severity of problem 2 by using simple estimates of how the undesigned loops will affect the output of the loop to be designed.

Problem 3 may affect the order of loop closing since we will require that the system is stable after the closing of each loop. Thus, it may not be possible to close the fast loop (k) first, if the corresponding transfer function element has a significant RHP zero that is not a transmission zero of the plant G. However, such RHP zeros in the individual elements of G may disappear when the other loops are closed (as the RHP zero is not a transmission zero), and it may therefore be possible to achieve fast control in loop k if the controller for this loop is designed at a later stage.

3. *Estimates of interactions*

In this section we use some simple facts to derive a priori estimates of the individual loop shapes (in terms of $g_{ii}c_i$), and show how this may be used to estimate the interactions caused by the undesigned loops.

3.1. *Bandwidth estimates*. We first derive estimates of the final loop shapes, and in particular, of the bandwidth in each loop. Note that all results given below assume that the inputs, outputs and disturbances have been scaled appropriately. In the more general case, weighting matrices may be used instead.

Consider the feedback system in Fig. 1. The control error (offset) is given by

$$e = y - r = -Sr + SG_d d. \tag{1}$$

Assume that the plant transfer function G and the disturbance transfer function G_d are scaled such that the largest tolerable offset (e) in any controlled variable has magnitude 1 and the largest individual disturbance (d) expected has magnitude 1 at any frequency. For simplicity we assume that the largest expected changes in the setpoints (r) are equal to the allowed magnitude of e. To satisfy our performance objectives, we must then for any single setpoint $|r_j| < 1$ at least require

$$|S_{ij}| < 1, \tag{2}$$

and for any single disturbance $|d_k| < 1$ at least require

$$|[SG_d]_{ik}| < 1. \tag{3}$$

(Here $[A]_{ij}$ denotes the ijth element of A.) We want to express these performance requirements in terms of the individual designs (loops).

A key step is to first factorize the sensitivity S in terms of the sensitivity of the individual designs, $\tilde{S} = (I + \tilde{G}C)^{-1}$ (e.g. Grosdidier and Morari, 1986):

$$S = (I + GC)^{-1} = \tilde{S}(I + E\tilde{H})^{-1}, \tag{4}$$

where $E = (G - \tilde{G})\tilde{G}^{-1}$ represents the relative interactions. For frequencies ($\omega < \omega_B$) below the bandwidths of the individual loops we have $\tilde{H} \approx I$ and we get $(I + E\tilde{H})^{-1} \approx \tilde{G}G^{-1} \stackrel{\text{def}}{=} \Gamma$. The control error becomes

$$e = y - r \approx -\tilde{S}\Gamma r + \tilde{S}\Gamma G_d d; \quad \omega < \omega_B \tag{5}$$

where $\Gamma = \{\gamma_{ij}\}$ is the Performance Relative Gain Array (PRGA) and $\Gamma G_d = \{\delta_{ik}\}$ is the Closed-loop Disturbance Gain (CLDG) (Skogestad and Hovd, 1990). At frequencies $\omega < \omega_B$ we also have $\tilde{S} \approx (\tilde{G}C)^{-1}$ and the performance requirements in equations (2) and (3) may then be rewritten in terms of bounds on the individual loop gains, $g_{ii}c_i$:

$$\text{Setpoints:} \quad \left|\frac{\gamma_{ij}}{g_{ii}c_i}\right| < 1 \Leftrightarrow |g_{ii}c_i| > |\gamma_{ij}|; \quad \omega < \omega_B \tag{6}$$

$$\text{Disturbances:} \quad \left|\frac{\delta_{ik}}{g_{ii}c_i}\right| < 1 \Leftrightarrow |g_{ii}c_i| > |\delta_{ik}|; \quad \omega < \omega_B. \tag{7}$$

Thus at frequencies $\omega < \omega_B$, the PRGA element $|\gamma_{ij}(j\omega)|$ is the minimum loop gain requirement for a change in setpoint j to cause an acceptably small offset in output i. Likewise, the CLDG element $|\delta_{ik}(j\omega)|$ is the minimum loop gain requirement in loop i for rejecting disturbance k. Specifically, from frequency-dependent plots of $|\gamma_{ij}|$ and $|\delta_{ik}|$, we can get a good estimate of the required bandwidth in the individual loops, ω_{Bi}. In the simplest case we may consider the frequency where the magnitudes $|\gamma_{ij}|$ or $|\delta_{ik}|$ cross one. In the example at the end of the paper we discuss a case where a more careful analysis is needed. The bandwidth estimates are later used for two purposes:

1. determine the order of loop closing (first closing loops that are required to be fast); and
2. estimate the complementary sensitivity functions ($\tilde{h}_i$) for the individual loops.

3.2. *Effect of undesigned loops*. The above relationships may be used to independently design each loop in terms of performance, at least at lower frequencies. However, when the controllers in some loops have already been designed, we have gained more knowledge about the closed-loop system, and we want to take advantage of this new knowledge when designing subsequent loops.

In the following, we will assume without loss of generality that the loops are closed (and controllers designed) in the order $1, 2, \ldots, k, k+1, \ldots,$ and that the loop to be designed is k. Let G_k denote the submatrix of dimension $k \times k$ in the upper left corner of G. Let $C_k = \text{diag}\{c_1, c_2, \ldots, c_k\}$ and let $S_k = (I + G_k C_k)^{-1}$ and $H_k = G_k C_k (I + G_k C_k)^{-1}$. Introduce $\hat{G}_k = \text{diag}\{G_k, g_{ii}\}$, $\hat{S}_k = \text{diag}\{S_k, \tilde{s}_i\}$, and $\hat{H}_k = \text{diag}\{H_k, \tilde{h}_i\}$, $i = k+1, k+2, \ldots, n$.

We then have the following generalization of equation (4):

$$S = \hat{S}_k (I + E_k \hat{H}_k)^{-1}; \quad E_k = (G - \hat{G}_k)\hat{G}_k^{-1}, \tag{8}$$

which is the basis for our design procedure. Note that:

1. $(I + E_k \hat{H}_k)^{-1}$ represents the estimated interactions from the undesigned loops;
2. to see this, note that $S_k = (I + G_k C_k)^{-1}$, the upper left $k \times k$ block of $\hat{S}_k$, yields the response for loops 1 to k with the remaining loops open, while the upper left $k \times k$ block of S yields the response of loops 1 to k with the remaining loops closed;
3. $(I + E_k \hat{H}_k)^{-1}$ is in general a full matrix. To evaluate this matrix we need an estimate of $\tilde{h}_i$ for the undesigned loops;
4. for $k = 1$ we have $\hat{G}_1 = \tilde{G}$, $\hat{S}_1 = \tilde{S}$, $E_1 = E$ and $\hat{H}_1 = \tilde{H}$ and rederive (4);
5. in our sequential design procedure we will consider the first k rows of $(I + E_k \hat{H}_k)^{-1}$ as an input weight when evaluating performance in terms of $S_k = (I + G_k C_k)^{-1}$; and
6. it is important to note that although we will take these estimated interactions $(I + E_k \hat{H}_k)^{-1}$ into account when evaluating performance, we will not take them into account when evaluating stability, during the design of loop k. The reason is that we will require the system to be stable after the closing of each loop.

4. *A new sequential design procedure*

The objective of the controller design is to design SISO controllers, c_i, that minimize some performance objective. As the performance objective we usually consider a norm (e.g. H_∞-norm or H_2-norm) of the weighted sensitivity function of the overall system, and get the following design problem:

$$\min_{c_i} \|W_P S W_D\|. \tag{9}$$

The performance weights $W_P^{n_P \times n}$ and $W_D^{n \times n_D}$ need not be square, but W_P is often a square diagonal matrix used to weigh each individual output e_i, that is, in most cases

$$W_P^{n \times n} = \text{diag}\{w_{P1}, w_{P2}, \ldots, w_{Pn}\}.$$

For a case where we consider both command following and disturbance rejection (see Fig. 1) the input weight is typically selected as

$$W_P^{n \times n_D} = [I \quad G_d].$$

Note that S can be expressed in terms of $\hat{S}_k$ as shown in equation (8). Obviously, we can only have a performance requirement for an output where we have a controller. For this reason, define

$$W_{Pk}^{n_P \times k}\text{: first } k \text{ columns of } W_P. \tag{10}$$

Likewise, define

$$W_{Dk}^{k \times n_D}\text{: first } k \text{ rows of } (I + E_k \hat{H}_k)^{-1} W_D. \tag{11}$$

Note that W_{Dk} includes the term $(I + E_k \hat{H}_k)^{-1}$ as an input weight to express the interactions from the undesigned loops.

4.1. *Summary of procedure.* Our proposed sequential design procedure is for step k to design a SISO controller c_k that minimizes $\|W_{Pk} S_k W_{Dk}\|$ where $S_k = (I + G_k C_k)^{-1}$ depends on c_k, and W_{Dk} is evaluated using an estimate of $\tilde{h}_i$ for $i \geq k$. At each step S_k is required to be stable. The main steps are as follows:

Step 0. Initialization. Determine the order of loop closing by estimating the required bandwidth in each loop. Also estimate the individual loop designs in terms of their complementary sensitivity $\tilde{H} = \text{diag}\{\tilde{h}\}$. For this step the loop gain requirements given in equations (6) and (7) in terms of the PRGA and CLDG are very helpful.

Step 1. Design of controller c_1 by considering output 1 only. We have $\hat{G}_k = \tilde{G} = \text{diag}\{g_{ii}\}$ and $\hat{H}_k = \tilde{H}$. W_{P1} is the first column of W_P, and W_{D1} is the first row of $(I + E_k \tilde{H})^{-1} W_D$.

Step k. Design of controller c_k by considering outputs 1 to k. Here $\hat{G}_k = \text{diag}\{G_k, g_{ii}\}$; $i = k+1, \ldots, n$. We use $\hat{H}_k = \text{diag}\{H_{k-1}, \tilde{h}_i\}$; $i = k, \ldots, n$, where H_{k-1} is the complementary sensitivity function for the $k-1$ loops that have been designed and $\tilde{h}_i$ is the estimate from Step 0 for the loops that are yet to be designed.

Step n. Design of the last controller c_n. This is done by considering the overall problem in (9).

4.2. *Remarks and discussion*

1. The design procedure may be generalized to cases where performance is defined in terms of closed-loop transfer functions other than S.
2. One objective with our procedure is that the use of the input weight W_{Dk} (using the estimate of $\tilde{h}_i$ for $i \geq k$) should reduce the need for iteration (redesigning loops), and this has indeed been confirmed by examples.
3. A choice has to be made as to what design method should be used for design of the SISO controllers. Alternatives are synthesis (with no restriction on the controller parametrization) and parametric optimization (with fixed controller parametrization). If we use an optimal design method, like H_2- or H_∞-synthesis, then the order of the controller c_k will increase for each step k. The reason is that for H_2- and H_∞-control, the order of the optimal controller equals the order of the plant including weights, and this order doubles for each step (this argument is used by Sandell *et al.* (1978) to justify that the optimal decentralized controller is infinite order since, in general, iteration is needed to find the optimal controller). We, therefore, prefer parameter optimization which yields simple low-order controllers, e.g. a PID-controller. The main disadvantage is that the achievable control quality depends on the controller parametrization.
4. With the possible exception of Step 0, the procedure is easily automated. One problem is that the parameter optimization, even though we consider only one controller at a time, is difficult and time-consuming. Typically, multiple local solutions may exist, and there is a need for research to find parametrizations where these problems are avoided.
5. With the exception of Step n, we propose to use the initial estimate of $\tilde{h}_k$ to evaluate $\hat{H}_k$ (and W_{Dk}) during the design of c_k, that is, we use $\hat{H}_k = \text{diag}\{H_{k-1}, \tilde{h}_i\}$ rather than $\hat{H}_k = \text{diag}\{H_k, \tilde{h}_i\}$. This is not strictly necessary, but it simplifies the problem set-up since $\hat{H}_k$ is then independent of c_k.
6. The limited degree of failure tolerance mentioned in Section 2 is guaranteed since S_k is required to be stable at each step in the design.
7. Because of this additional requirement that the system is stable after closing each loop, it is not possible, in general, to obtain the optimal decentralized controller by sequential design. However, for the examples we have studied, our procedure achieved a control quality almost equivalent to that achieved using parameter optimization for all loops simultaneously.
8. Although our design procedure is new, the idea of using a simplified estimate of the effect of closing the other loops is not new. For example, Balchen and Mummé (1988, Appendix C) derive an estimate for the transfer function in loop k using an estimate of $\tilde{h}_i$ for the other loops, and use this to find pairings.
9. It is easier to estimate the complementary sensitivity function for the individual loops than to estimate the controller in the individual loops. This holds especially at low frequency, where control is almost perfect, and we know that $\tilde{h}_i \approx 1$.
10. In the example we use an H_∞ performance objective,

$$\|W_P S W_D\| = \|W_P S W_D\|_\infty = \sup_\omega \bar{\sigma}(W_P S W_D). \tag{12}$$

In the example we also include model uncertainty, and to satisfy robust performance (RP) the requirement

$\|W_P S W_D\|_\infty < 1$ should be satisfied for all possible values of S allowed for by the uncertainty description. With H_∞-bounded model uncertainty this may be reformulated as an equivalent structured singular value test. For example, for the case with multiplicative input uncertainty (see Fig. 2) we get the robust performance condition (e.g. Skogestad and Morari, 1989)

$$\mu_\Delta \begin{bmatrix} W_I CSG & W_I CSW_D \\ W_P SG & W_P SW_D \end{bmatrix} < 1, \quad \forall \omega, \qquad (13)$$

where μ is the structured singular value (Doyle *et al.*, 1982) and $\Delta = \mathrm{diag}\{\Delta_I, \Delta_P\}$. Δ_I is a diagonal matrix representing the input uncertainty, and Δ_P is a full matrix representing the performance requirement. Our sequential design procedure is then for step k to design a SISO controller that minimizes

$$\mu_{\Delta_k} \begin{bmatrix} W_{Ik} C_k S_k G_k & W_{Ik} C_k S_k W_{Dk} \\ W_{Pk} S_k G_k & W_{Pk} S_k W_{Dk} \end{bmatrix}. \qquad (14)$$

with $\Delta_k = \mathrm{diag}\{\Delta_{Ik}, \Delta_P\}$. Here Δ_{Ik} a diagonal $k \times k$ matrix and Δ_P is a full $n_D \times n_P$ matrix.

5. *Example*

We shall here consider an example from Chiu (1991). The plant is given by

$$G(s) = \begin{bmatrix} \dfrac{0.66}{6.7s+1} & \dfrac{-0.61}{8.4s+1} & \dfrac{-0.005}{9.06s+1} \\ \dfrac{1.11}{3.25s+1} & \dfrac{-2.36}{5s+1} & \dfrac{-0.01}{7.09s+1} \\ \dfrac{-34.7}{8.15s+1} & \dfrac{46.2}{10.9s+1} & \dfrac{0.87(11.61s+1)}{(3.89s+1)(18.8s+1)} \end{bmatrix} \qquad (15)$$

The outputs are assumed to be scaled correctly with respect to each other. We immediately note the strong one-way interaction in the system represented by the large off-diagonal elements in row three. In Chiu (1991) only robust stability is considered, with independent, multiplicative input uncertainty (see Fig. 2) with uncertainty weight $W_I(s) = 0.13\dfrac{5s+1}{0.25s+1}I$. This uncertainty weight reflects a steady state gain uncertainty of 13% and a maximum neglected time delay of 0.5 min. We add the performance requirement $\bar{\sigma}(W_P S) < 1$, $\forall\omega$, which should be satisfied for all possible plants allowed by the input uncertainty. We choose the performance weights

$$W_D = I; \quad W_P = w_P I; \quad w_P(s) = 0.4\frac{\tau_{cl}s+1}{\tau_{cl}}. \qquad (16)$$

The objective is to make the system as fast as possible in a robust sense, by minimizing τ_{cl} in the performance weight subject to $\mu_{RP}(M) < 1$ (μ_{RP} meaning μ for robust performance), where M is as given in equation (13).

We follow Chiu (1991) and choose to pair on the diagonal elements of G. We first want to estimate the required bandwidth, ω_{Bi}, in each loop.

The PRGA for this example is shown in Fig. 3 (solid lines), together with the uncertainty weight (dashed lines). PRGA elements larger than 1 imply interactions, and the figure shows that there is, as expected, severe interaction from loops 1 and 2 into loop 3. The loop gain in loop 3 must consequently be high at the frequencies where the feedback in loops 1 and 2 are effective to reject the 'disturbances' entering from loops 1 and 2. This means that the bandwidth in loop 3 has to be higher than the bandwidth in loops 1 and 2.

The bandwidth in loop 3 will be limited by the time delay

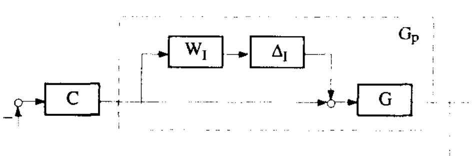

FIG. 2. Multiplicative input uncertainty.

of 0.5 min allowed by the input uncertainty. We therefore estimate $\omega_{B13} = 1$ [rad/min], which is slightly below the frequency where the input uncertainty weight, $|W_I|$, crosses one.

Next consider the 'disturbance' from loop 1 into loop 3, as expressed by the PRGA element γ_{31}. We have $\gamma_{31} \approx 50$ for frequencies lower than approximately 0.1 [rad/min]. Thus, at the bandwidth frequency for loop 1, ω_{B1}, we must from equation (6) require $|g_{33}c_3(j\omega_{B1})| > \gamma_{31}(j\omega_{B1}) = 50$. If $|g_{33}c_3|$ has a slope of $-p$ on the log-log Bode magnitude plot, this yields $(\omega_{B2}/\omega_{B1})^p > |\gamma_{31}(j\omega_{B1})|$. For $p = 2$ (i.e. 40 dB/decade) and $\omega_{B2} = 1$ [rad/min] we get $\omega_{B1} < 1/\sqrt{|\gamma_{31}|} = 1/7.1$ [rad/min] (7.1 min is then the best response time we can have for loop 1, since in practice the slope for loop 2 will be less than -2). A similar discussion applies for the interaction from loop 2 into loop 3. We have $|\gamma_{32}| \approx 10$ at low frequencies, and if we assume that loop 3 has a slope -2 in the frequency region between ω_{B1} and ω_{B2} (which indeed turns out to be correct for our design), then for the interactions of loop 1 and loop 2 into loop 3 to be of equal significance, we get $\omega_{B2}/\omega_{B1} = \sqrt{|\gamma_{31}|/|\gamma_{32}|} \approx 2.2$, which is used in the following.

From the above discussion the controller parametrization is chosen to allow a high roll-off

$$c_i(s) = k\frac{T_1 s+1}{T_1 s}\frac{T_2 s+1}{10T_2 s+1}. \qquad (17)$$

Note that this is not a PID controller since the pole in the last term is at a lower frequency ($s = 0.1/T_2$) than the zero.

We have now obtained sufficient information to proceed with our design procedure.

Step 0. From the above discussion we conclude that the order of loop closing should be: loop 3 (fastest), loop 2, loop 1. The initial estimates for the complementary sensitivity functions for the individual loops are chosen to be second order of the form

$$\tilde{h}_i(s) = \frac{1}{\left(\dfrac{s}{\omega_{Bi}}+1\right)^2}. \qquad (18)$$

As estimates of the loop bandwidths ω_{B1}, ω_{B2} and ω_{B3}, we select based on the above discussion the following:

1. loop 3 is the fastest and we estimate $\omega_{B3} = 1$ [rad/min];
2. $\omega_{B2}/\omega_{B1} \approx 2.2$;
3. $\omega_{B1} = 1/\tau_{cl}$ where τ_{cl} is minimized at each step such that $\mu = 1$. This choice follows since loop 1 is the slowest loop, and has little interactions from the other loops. Thus the response of this loop by itself will determine the performance of the overall system.

Step 1. Controller design for loop 3. W_{D1} is the third row of $(I + E_k\hat{H}_k)^{-1}$, and there is one 1×1 perturbation block for the input uncertainty, and one 3×1 perturbation block for the performance specification. Iterating on τ_{cl} (and changing ω_{B1} and ω_{B2} correspondingly, as explained above) we obtain $\mu = 1.0$ for $\tau_{cl} = 8.5$ (min), and the corresponding controller is

$$c_3(s) = 84.9\frac{4.70s+1}{4.70s}\frac{4.01s+1}{40.1s+1}. \qquad (19)$$

Step 2. Loop 2. In $\hat{H}_k$ we replace the estimate of $\tilde{h}_3$ by the actual design for loop 3. W_{D2} is the second and third row of $(I + E_k\hat{H}_k)^{-1}$. There is one diagonal perturbation block of dimension 2×2 for the input uncertainty, and a 3×2 perturbation block for performance. $\mu = 1.0$ is obtained for $\tau_{cl} = 11$ (min), with

$$c_2(s) = -0.079\frac{1.32s+1}{1.32s}\frac{0.186s+1}{1.86s+1}. \qquad (20)$$

Step 3. Loop 1. Now all loops are included and we consider the overall design problem with a diagonal 3×3 perturbation block for the input uncertainty and a full 3×3 perturbation block for performance. $\mu = 1.0$ is obtained for $\tau_{cl} = 18$ (min) with

$$c_1(s) = 0.94\frac{0.385s+1}{0.385s}\frac{0.898s+1}{8.98s+1}. \qquad (21)$$

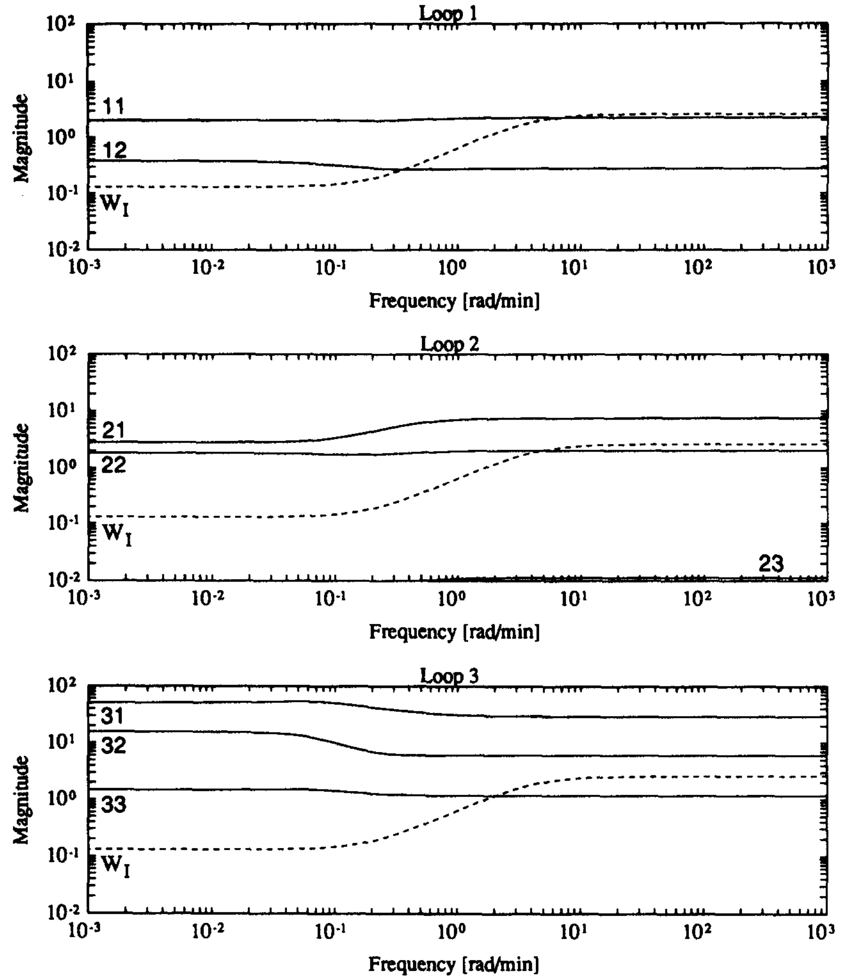

FIG. 3. Elements of PRGA = $\tilde{G}G^{-1}$ (solid lines) and uncertainty weight (dashed line). $PRGA_{13}$ is smaller than 10^{-2} at all frequencies.

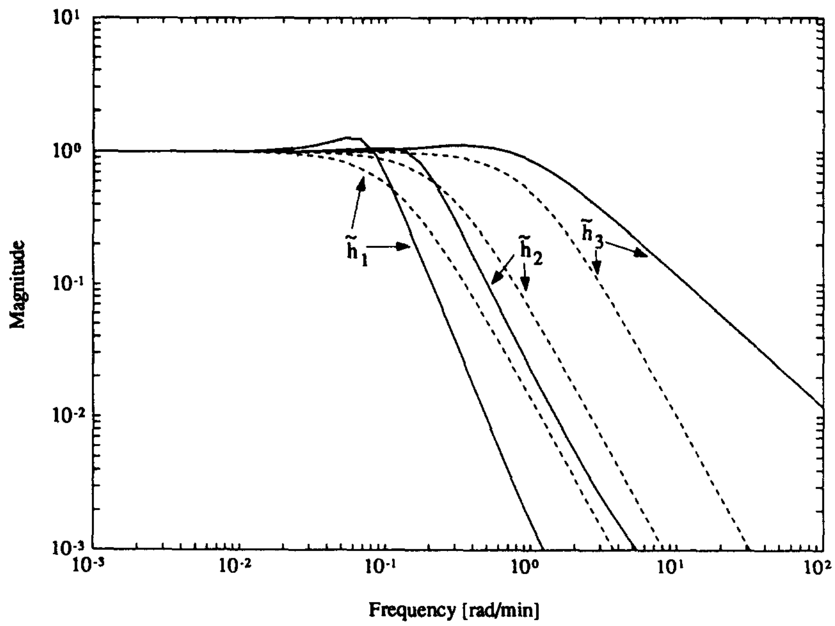

FIG. 4. Complementary sensitivity functions for the individual loops, $\tilde{h}_i$. Solid: final designs. Dashed: estimates at Step 1 of the design ($\omega_{B1} = 1/8.5$, $\omega_{B2} = 2.2\omega_{B1}$, $\omega_{B3} = 1$).

Note that τ_{cl}, which was obtained in the last step, is the value of τ_{cl} which will apply to all outputs in the overall problem. In comparison, the best decentralized controller found using simultaneous parametric optimization with the same controller parametrization in equation (17) gave $\mu = 1$ for $\tau_{cl} = 16$ (min). This demonstrates that there is little to be gained by iterating on the design.

The final complementary sensitivity functions (solid lines) for the individual loops, $\tilde{h}_i$ are shown in Fig. 4, together with the estimates (dashed lines) used in Step 1 of the design. These differ considerably, and this illustrates that the design method does not require very accurate a priori estimates of $\tilde{h}_i$.

In Fig. 5(a) we show the response to a unit setpoint change in output 1 (the most difficult direction). The interactions are pronounced, but acceptable. As seen from the dashed lines the responses are insensitive to adding 0.5 min time delay in all channels.

5.1. *Comparision with conventional design.* For this example, conventional sequential design, e.g. based on Ziegler–Nichols tunings, will yield unacceptable designs, because conventional sequential design only considers one output at a time. Thus, there is no incentive for restricting the bandwidths of loops 1 and 2 in order to avoid interactions into loop 3. This is seen from the simulations in Fig. 5(b) where we use the BLT PI-tunings of Luyben (1986) (Table 1), which are based on detuning the Ziegler–Nichols tunings by a common factor for all loops.

Note that although the BLT PI controller is found to perform poorly on this example, there does exist a decentralized PI controller with almost as good a robust performance as the controller obtained using the proposed sequential design procedure. For $\tau_{cl} = 18$ (min) we obtained by simultaneous parameter optimization PI-tunings (0.032, 0.26 min; −0.044, 1.01 min; 9.30, 2.36 min) which gave $\mu_{RP} = 1.08$.

5.2. *Other examples.* In the thesis by Hovd (1992) our sequential design procedure is applied to the open-loop unstable 3 × 3 polypropylene reactor example presented by Lie and Balchen (1992). In the example, disturbances are important and the CLDG is used to estimate the loop gain requirements. The example has no multivariable RHP zeros, but presence of RHP zeros in the individual element makes it necessary to design the fastest loop last. We find also for this

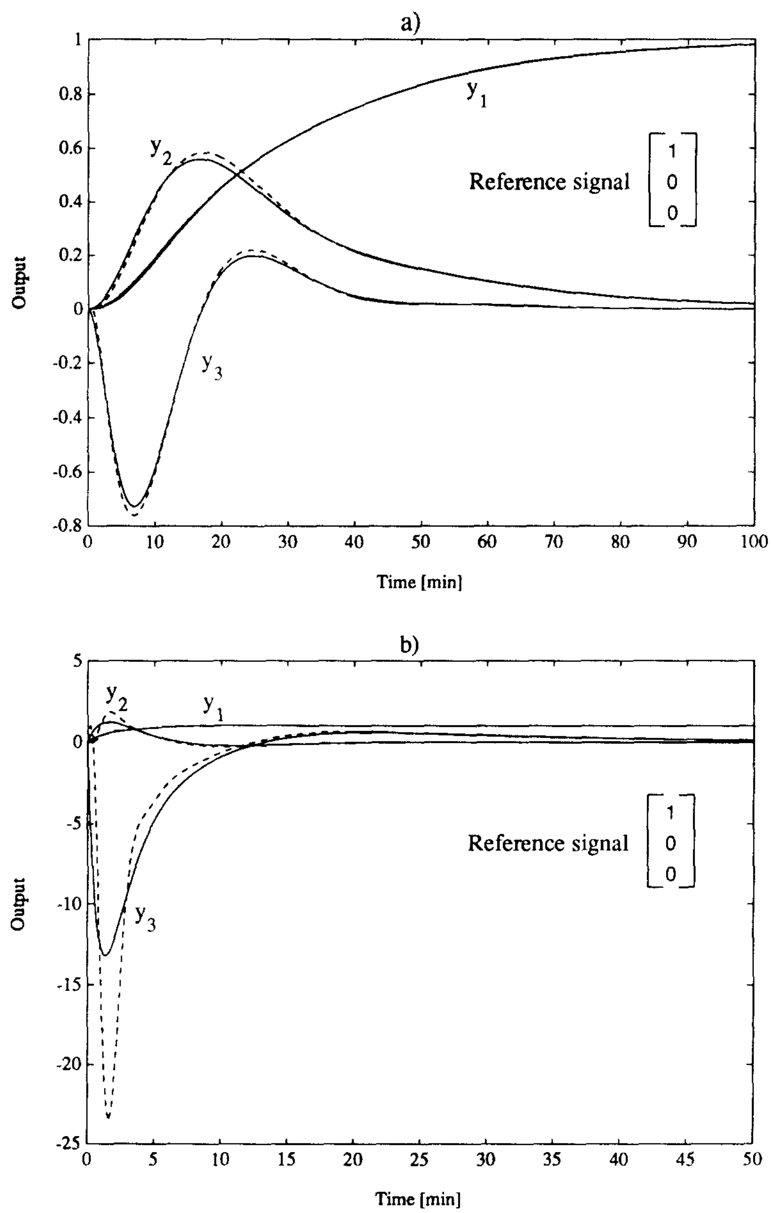

FIG. 5. Responses with decentralized control. (a) Sequential design. (b) BLT-detuned Ziegler–Nichols PI-tunings (note scale on y-axis). Solid: nominal responses. Dashed: 0.5 min time delay on inputs.

TABLE 1. ZIEGLER–NICHOLS PI TUNING FOR EXAMPLE (FOR THE LOOPS TUNED INDEPENDENTLY). THE BLT PI CONTROLLER HAS GAIN k_i/f AND INTEGRAL TIME CONSTANT $T_i f$

Loop	k_i	T_i
1	14.75	1.65
2	−3.11	1.64
3	10.71	1.63
BLT detuning factor: $f = 2.23$		

example that our sequential design procedure yields results which are only marginally different to those obtained by simultaneous design of all controllers.

6. *Conclusion*

We propose a new sequential design procedure that involves minimizing the performance criterion at each design step. The key basis for our design procedure is the factorization of the overall system in terms of the individual designs (equations (8)), and the use of estimates for the complementary sensitivity functions ($\tilde{h}_i$) of the loops that are yet to be designed. By use of equations (6) and (7), which use the PRGA and CLDG to quantify the interactions for setpoint tracking and disturbance rejection, we are able to obtain good initial estimates of the required loop gains ($g_{ii}c_i$), and thus estimate the required bandwidth in each loop (ω_{Bi}), which in turn is used to estimate $\tilde{h}_i$ (e.g. see equation (18)).

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